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CONDUCTIVITY MODULATION IN CR/CRYST.-SI MS STRUCTURE STUDIED THROUGH CURRENT-VOLTAGE AND ADMITTANCE MEASUREMENTS

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ABSTRACT

Temperature dependent a.c. capacitance (C) together with ac conductance(G/ω) under various frequency (ω) and d.c. current (I) measurements as a function of bias (V) were employed to investigate both majority and minority carrier injection phenomenon on chromium- p type crystalline silicon (Cr/p-cryst. Si) Schottky diode. This ambipolar transport process behaved differently according to the mentioned techniques: under forward bias, there was a increase in capacitance towards maximum while majority carrier injection proceed from the back electrode. Meanwhile, minority carrier injection from front electrode cause to sharp decrease in measured capacitance from peak position, leading to observation a hump in C-V analysis and followed up tendency due might be interface states and finally end up with constancy. Moreover, shape and peak position of the hump had both frequency and temperature dependency. Remarkably, in the bias range where hump observed, space charge limited current (SCLC) was discerned as the actual enrolled current flow mechanism in I-V measurement, confirming further majority carrier injection. In addition, both dc conductivity and ac conductance behaved similarly. On the other side, reverse current was proportional to square root of reverse bias where constancy of capacitance appeared. These experimental identifications simply imposed the existence of conductivity modulation issue in metal-semiconductor (MS) junction which relies on majority carriers and mostly minority carrier injection is disregarded.
Keywords: Conductivity modulation, minority carrier injection.
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CR/P-Sİ MS YAPISINDAKİ İLETKENLİK MODÜLASYONUNUN AKIM-GERİLİM VE ADMİTTANS ÖLÇÜMLERİYLE İNCELENMESİ

ÖZET

Sıcaklığa bağlı faklı frekanslardaki ac sığa ile birlikte ac iletkenlik ve dc akım ölçümleri, gerilimin fonksiyonu olarak krom-p tipi silisyum yariletkenden oluşmuş MS yapısında, çoğunluk ve azınlık yük enjeksiyon olgusunu incelemek üzere kullanıldı. Ambipolar yük taşınması, bahsedilen tekniklere göre farklı davranışlar sergilediği ortaya çıkarıldı; şöyle ki düz beslemede ölçülen sığa değeri, gerilim ile artarak maksimum noktasına ulaştı. Bu durum, arka elektrotdan çoğunluk yüklerin enjeksiyonu olarak yorumlandı. Aynı zamanda, belirli bir gerilimden sonra, ön elektrotdan sızan azınlık yükleri ise, tepe noktasına ulaşmış sığa değerinin azalması olarak C-V eğrilerinde kendini gösterdi. Sonuçta, düz gerilimin şiddetine göre, artarak bir tepecikten geçen ve sonrasında azalan bir C-V davranışı gözlemlendi. Üstelik, tepeciğin şeklinin ve tepe noktasının frekans ile değiştiği anlaşıldı. Tepeciğe karşılık gelen gerilim aralığında, uzay yük sınırlamalı akım mekanizmasının başat olduğu ölçülen akım –gerilim eğrileri incelerek ortaya konuldu. Dahası, hem dc iletkenliğin hem de ac iletkenliğin benzer davranışlar sergilediği gözlenildi. Öte yandan, ters beslemedeki akım şiddetinin, ters gerilimin karekökü ile orantılı olduğu bulundu. Bu deneyse gözlemler, sıklıkla etkileri ihmal edilen ve çoğunluk yük taşıyıcılarının başat olduğu bilinen MS yapısında azınlık yüklerden kaynaklı iletkenlik modülasyonunun gerçekleştiği savını güçlendirdi.
Anahtar Sözcükler: İletkenlik modülasyonu, azınlı yük enjeksiyonu.

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1. INTRODUCTION

Metal-semiconductor (MS) junction relies on majority carriers where mostly minority carrier injection is disregarded. However, in some cases, unappreciated this issue play a key role where injection of electrons into p-type crystalline silicon (p-c-Si) from the metal electrode could not be negligible at high forward biases and becomes significant in surveying techniques; namely current-voltage (I-V) and admittance ($Y= G_m+j\omega C_m$ where G_m= ac conductance and C_m= capacitance) measurements, respectively. In other words, electrons are injected from the metal side whilst holes are injected from the semiconductor and hence bipolar (ambipolar) transport process occur in Schottky diode. To do so, barrier height (Φ) for electrons (minority carriers) should be low while the barrier height for holes (majority carriers) must be high and sum of them shall be equal to energy band gap (E_G) of semiconductor. In the case of $\Phi>E_G/2$, injection usually takes place and produce inversion layer where minority carriers exceed majority ones (n>p). Under the appropriate bias application, some of these injected minorities diffuse towards neutral region of semiconductor whilst equal amount of opposite majorities should enter from the back electrode to maintain charge neutrality. Consequently, modulation of conductivity occurs and manifest itself as reducing diode series resistance (R_s) and improves rectification ratio (forward current/reverse current) in I-V measurement [1-2]. For the admittance measurement, on the other hand, diffusion of minority carriers strongly affected C_m together with G_m (as in the case of dc conductivity) behavior on the forward bias (accumulating type bias), especially at low frequency. Equivalently, while bias is scanned under low frequency in the C-V measurement, the capacitance increases until a point where it reaches maxima and decreases sharply afterwards.That is there would be a hump whose shape and position depends on bulk resistivity and nature of the metal contacts [3-6]. Besides, maxima of the hump decreases with increase in both frequency and forward bias.

In this work, MS junction was produced to study minority carrier injection issue through I-V in conjunction with $C_m(G_m/\omega)$-V measurements.

2. EXPERIMENTAL

(100) oriented boron doped p type silicon wafer (1-3 Ω cm) was cleaned with standard RCA cleaning procedure. Prior to placing the substrate, backside of it was coated by aluminum (Al) and the sample was annealed in nitrogen ambient at 530 ^oC to form ohmic contact. After coating, metal/p-Si/metal structure was fabricated by evaporation of chromium (Cr) gate electrode through a shadow mask of diameter 0.11 cm by e-beam deposition system. I-V and $C(G/\omega)$-V_G characteristics were reported at room temperature in evacuated cryostat in dark condition via Keithley 6517 multimeter and HP4192A LCR meter, respectively. Experiments were performed through a LABVIEW program.

3. EXPERIMENTAL RESULTS

a) I-V Characteristic of Cr/p-Si junction

Figure 1 depicted I vs. V variation for an Cr/p-Si MS juction under forward and reverse direction at room temperature. As clearly seen, the current seemed higher in forward direction than in the reverse one; implying rectfying property. This diode characteristic was thought to the barrier existing between metal and semiconductor when brought into intimate contact. Consequently, barrier height (Φ) and ideality factor (n) of the MS structure were obtained as 0.84 eV and 1.3, respectively. Moreover, along the I-V curve in forward direction , the initial linear (ohmic) region, was followed by a superlinear region ($I \sim V^{p}$ where p, inversely varying with temperature[7], was located as 3.3 at room temperature (300 K). This power law dependence of

the current on the applied voltage beyond a critical value might be possibly due to a space charge limitation (SCL). In the reverse direction, on the other hand, current was proportional to the square root of reverse applied bias, indicating a depletion layer as expected for the MS structure at hand.

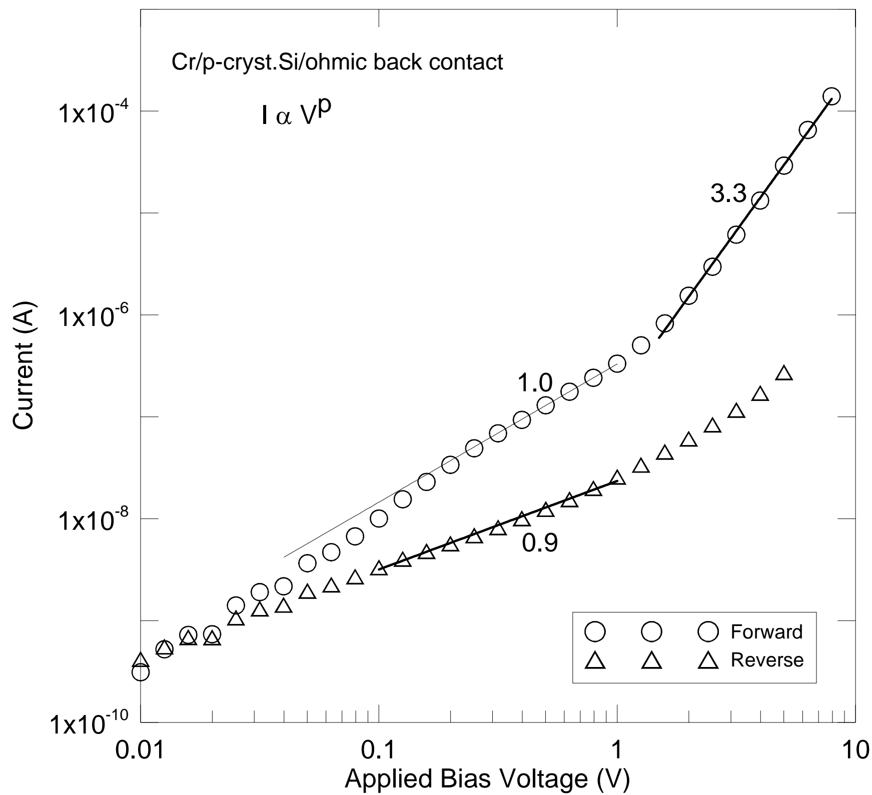
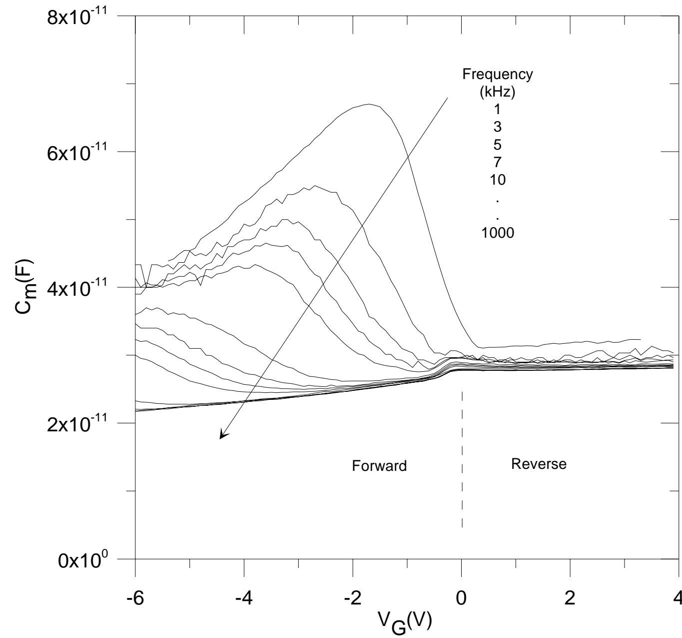


Figure 1. I versus V variation for an Cr/p-Si MS junction at room temperature under forward and reverse directions

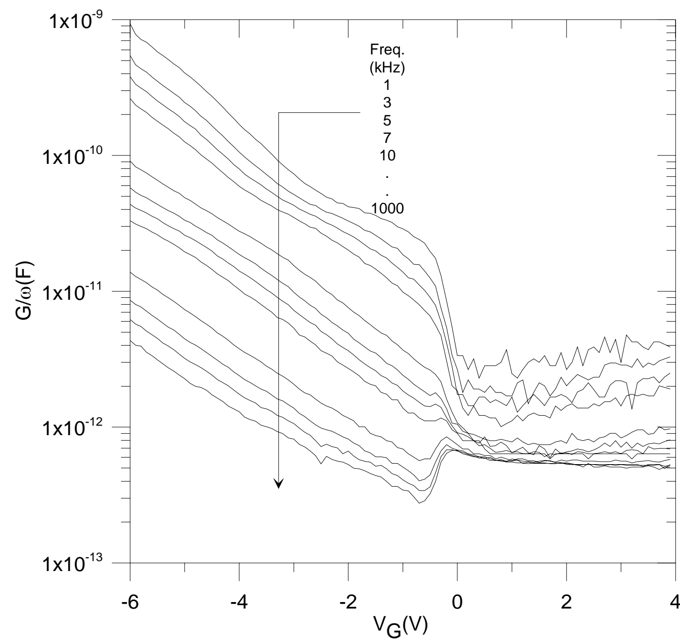
b) Admittance Analysis of Cr/p-Si junction

Both capacitance (C_m) and conductance (G_m/ω) variations of the MS structure as a function of dc gate bias voltage V_G for various ac modulation frequencies were given in Figure 2. Apart from almost expected voltage behavior, there was remarkably strong frequency dependence. As clearly seen in figure 2-a, capacitance of the structure increased drastically at a certain amount of forward bias and then begun to decline after reaching a maximum value. Moreover, the increase was more pronounced under relatively low ac modulation frequency (1kHz in here). In addition, it was reported that onset voltage of the increase in capacitance depended on the metal used as gate electrode [3-6]. On the other hand, from positive to zero gate bias, there was no remarkable change in capacitance.

The variation of the conductance with bias of Cr/p-c-Si Schottky diode at different frequencies was shown in figure 2-b. The conductance data have been given for completeness and comparison with the d.c. conductivity, discussed in subsequent section.



(a)



(b)

Figure 2. (a) Capacitance (C_m) and (b) conductance (G_m/ω) variations of the MS structure as a function of dc gate bias voltage V_G for various a.c. modulation frequencies (1kHz-1MHz) at room temperature

4. DISCUSSION

Comparison of I-V and $C_m(G_m/\omega)$-V_G curves (given in fig.1 and fig.2) exhibited majority and minority carrier injection phenomenon. As depicted in figure 2-a, the capacitance of the structure increased in forward bias until a point where it reaches a maxima and then sharp decrease was eventual. Whenever majority carrier injection begun, a sharp rise in capacitance took place. When the bias was kept to increase in further, minority carrier injectin started over and marked a decrease in measured capacitance after passing through the maxima. The decrease in capacitance could also be interpreted as not only due to the neutralization of trapped charges but also owing to the recombination processes of injected holes and electrons in the depletion layer of MS structure (see figure 3). Once the current compared with the capacitance, the similar issue manifested itself in a specific bias voltage interval, as illustrated in figure 3; onset voltage of increase in capacitance corresponded to the beginning of SCL current mechanism and maximum point in capacitance reflected to the bias value where minority carrier injection starts over. Also, both d.c. conductivity and a.c. conductance behaved similarly with nearly the same magnitude. This was predictacle since barrier height for holes is 0.84 eV whilst for electrons 0.28 eV, fulfilled the condition of injection processes. Therefore, injected electrons due to forward bias produced inversion layer where n>p, and some of them diffuse towards neutral region of semiconductor under relatively large forward bias condition. In the mean time, equal amount of holes should be supplied from the back electrode to maintain charge neutrality, resulting increase in conductivity.

Descriptive model based on transport feature as to I-V measurement on MS structure can be interpreted in C-V measurement as follows: provided that minority carrier concentrations become comparable with the equilibrium concentration $(n \approx N_A)$, storage type behavior turnes into inductive type which can also be interpreted as negative capacitance. The inductive contribution, in other words, modulation of series resistance due to hole injection, necessitate time and hence delay between the applied voltage and ac current take place. Therefore, once C becomes inductive, the forward bias voltage reflects the inversion voltage where $n > p$ and hence temperature/frequency dependence is expected and experimentally depicted in figure 2-a. Eventually, the inductive contibution gets weaker under high frequency (or low temperature) as illustrated in figure 2-a due to the fact that minority carriers can not follow such high ac voltage modulation

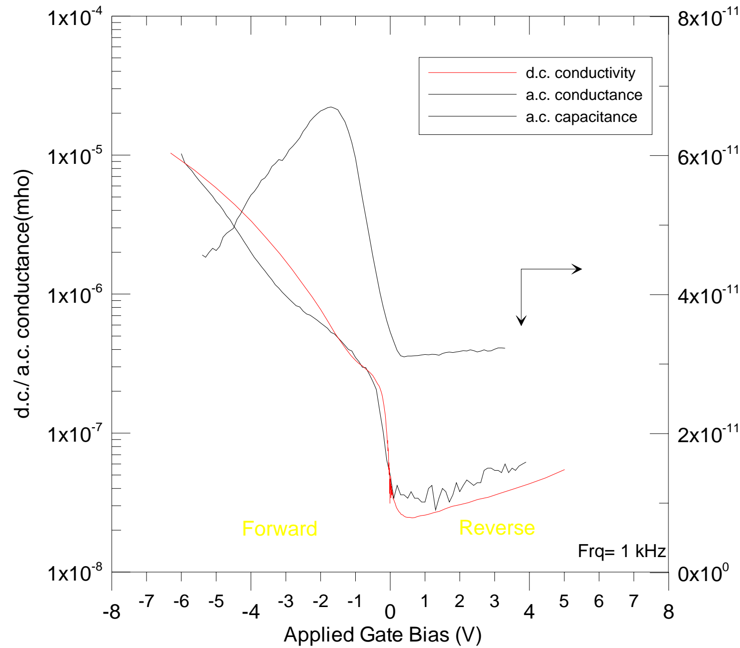


Figure 3. A representative 1 kHz C-V curve under reverse and forward bias voltages to depict distinct regions corresponding to the amount of charge injected into p-c-Si from electrodes. Also, d.c. conductivity and a.c. conductance data were demonstrated within the same graph to relate between charge injection and its corresponding capacitance behavior.

5. CONCLUSION

Majority and minority carrier injection took place in the forward direction in a specific bias voltage interval; onset voltage value marked the majority carrier injection where sharp rise in capacitance was eventual whereas decrease in measured capacitance (after passing maxima) denoted the associated voltage where minority carrier injection begun.

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