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Research Article

A novel Bulk-driven current differential transconductance amplifier and its applications

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ABSTRACT

This research proposes a novel, more efficient bulk-driven current differential transconductance amplifier (BDCDTA) for low-voltage, low-power applications. The proposed design consists of a current difference unit followed by a transconductance amplifier, which utilizes a split transistor network approach to obtain high transconductance. In the biasing circuit, a current source and a split network are also incorporated, allowing the BDCDTA characteristics to be tuned as needed by properly selecting its value and the number of transistors. To demonstrate the capabilities of the proposed BDCDTA, a biquad filter is constructed. Furthermore, as a new BDCDTA application, frequency agile filters are also implemented. The frequency-agile filter, which has only three active elements, is simple to integrate, and the center frequency can easily be electronically adjusted by changing the bias current amount. The simulations are performed using PSPICE 180 nm CMOS technology parameters. All calculations and simulated outcomes validate the overall performance and potential of the presented circuit and its applications.

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INTRODUCTION

The current differential transconductance amplifier (CDTA) is a current mode active element that was initially introduced in 2005 [1], and the first CMOS implementation was provided in [2]. Later, other authors proposed various methods for its implementation [3-5]. According to [6], this basic CDTA block has been extensively utilized in a variety of applications, including filters [7-12], rectifiers [13], oscillators [14-17], modulators [18], multipliers [19, 21-23], memristor emulator [20], square-rooters, squarer [21], Schmitt trigger [22], and divider [21, 23]. It confirms the versatility of this device for its extensive use.

Downscaling complementary metal oxide semiconductor (CMOS) devices led to developments in smaller integrated circuits (ICs). As a result, active elements capable of operating at low supply voltages with considerably less power dissipation are required. According to the literature, the following approaches are commonly used for this purpose: sub-threshold, floating gate, quasi-floating gate [7, 8], and bulk-driven [24-32]. As a result, following the concept of basic CDTA, bulk-driven CDTA (BDCDTA) was introduced in 2011 [26].

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The bulk-driven approach has an important advantage of low power consumption and operating voltage. It also takes up less chip space than other techniques because it has fewer transistors and a lower associated capacitance value [27]. Still, because it has less transconductance than conventional metal oxide semiconductor field effect transistor (MOSFET), it has much less gain bandwidth product [28]. Probably due to this reason, not many implementations and corresponding applications using BDCDTA could be proposed to date.

To make the BDCDTA practical and demonstrate its applicability in more applications, its transconductance and frequency response must be increased. For this reason, we presented a novel BDCDTA design based on a transconductance boosting approach [4], which can be effectively customized to get the desired results. Furthermore, we have presented a new application for this novel BDCDTA, namely the frequency agile filter, which was not in a position to be designed with the conventional one.

Our work is presented here in the following manner: Section 2 begins with the basic BDCDTA concept as well as its characteristics described in [26]. Section 3 depicts the proposed BDCDTA, while Section 4 elaborates on the simulation results, discussion, and performance comparison. The suggested BDCDTA's use in the biquad filter is explored in section 5, and its usage in the frequency agile filter is explained in section 6, which proves the versatility of our proposed design. Finally, concluding remarks are covered in section 7 which also incorporates future possibilities.

BDCDTA Symbol and its Characteristics

Figure 1 depicts the BDCDTA schematic symbol, which was introduced in 2011 [26]. It has three bulk-driven OTAs in all, the first two of which are used to determine the difference between the applied input currents and the third of which is employed to produce sufficient transconductance gain. This also includes an external resistor R_{set} which sets but also limits the transconductance of the BDCDTA with a value of $g_{mset} = 1/R_{set}$.

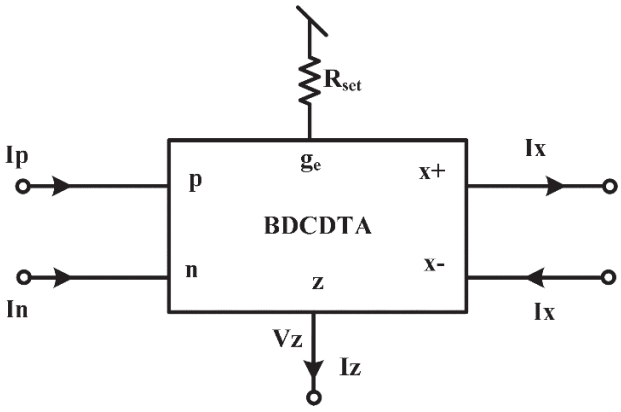

Figure 1. The schematic symbol of BDCDTA [26].

The following set of equations describes the characteristics of the BDCDTA-

$$I_z = \Delta I = I_p - I_n$$
$$V_p = V_n = 0 \quad (1)$$
$$I_{x+} = g_{mb} V_z \text{ and } I_{x-} = -g_{mb} V_z$$

where g_{mb} is the transconductance of bulk-driven OTA. Furthermore, an external resistance R_z connected to the 'z' terminal converts the current I_z into an equivalent voltage V_z, which is required to drive the third OTA and deliver the output current I_x.

Proposed Performance-Enhanced BDCDTA

The proposed BDCDTA circuit

Figure 2 provides the schematic diagram for the proposed BDCDTA. It has two bulk-driven CCIIs, which are made up of bulk-driven OTAs to form the bulk-driven current differential unit. Following that, there is an upgraded bulk-driven OTA network, which is primarily responsible for producing the necessary transconductance gain.

For the first BDCCII, the applied current Ip moves from its 'z-' terminal, and for the next BDCCII the current I_n moves towards its 'z_+' terminal, hence both are in the opposite direction. As a result, the current detected at the BDCDTA's 'z' terminal is simply the difference between the two currents, I_p and I_n.

Here, the function of the third OTA is to provide sufficient gain but due to bulk mode, its transconductance (g_{mb}) is naturally much lower than its conventional counterpart (g_m) as described by equation (2).

$$g_{mb} = \eta\, g_m \quad (2)$$

with $\eta = \frac{\gamma_p}{2\sqrt{V_{BS} + 2\emptyset_f}}$

where, γ_p is a constant describing the substrate bias effect, V_{BS} is bulk to source potential of the transistor and φ_f is the fermi potential of the bulk terminal. Based upon the typical values of the above parameters, it is found that the value of η comes out to be approximately between 0.2 and 0.4, which elucidates that the value of bulk mode transconductance is less with this factor in comparison to the transconductance of the conventional MOSFET.

Due to this restriction, a single bulk-driven transistor is insufficient to provide a higher transconductance value. Therefore, to improve its value we have used a split transistor network approach in the OTA section as shown in Figure 3.

A split transistor network utilizes 'n' MOSFETs in parallel instead of a single transistor. All transistors will have the same current flowing through them since they all have the same potential. Therefore, the current at the drain terminal will be the sum of all the individual transistor currents and hence the output current is multiplied by 'n' times. However, due to integrated circuit fabrication area

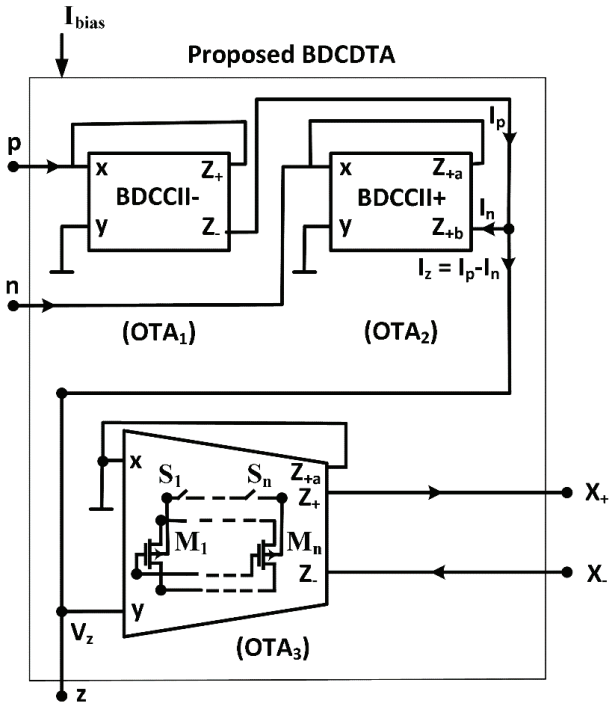

Figure 2. Schematic diagram of proposed BDCDTA.

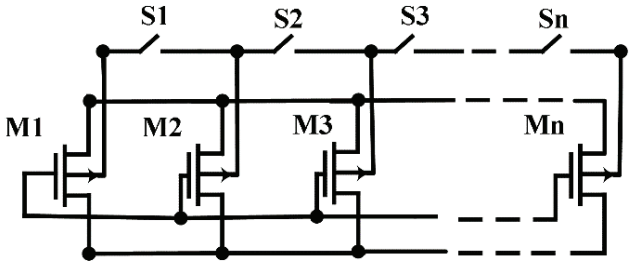

Figure 3. Split transistor network approach used in the proposed BDCDTA.

limitation and increased associated capacitance values, size can't be increased arbitrarily. However, further analysis of the circuit reveals that employing such a network with a proper aspect ratio can boost total current, transconductance, and bandwidth.

The value of the current I_D for the bulk-driven MOS of Figure 3 can be obtained from equation (3)-

$$I_D = \frac{\beta}{2}\{V_{SG} - V_{TP0} - \gamma_p\left(\sqrt{V_{BS} + 2\emptyset_f} - \sqrt{2\emptyset_f}\right)\}^2 \qquad (3)$$

with $\beta = \mu_p C_{ox} \frac{W}{L}$

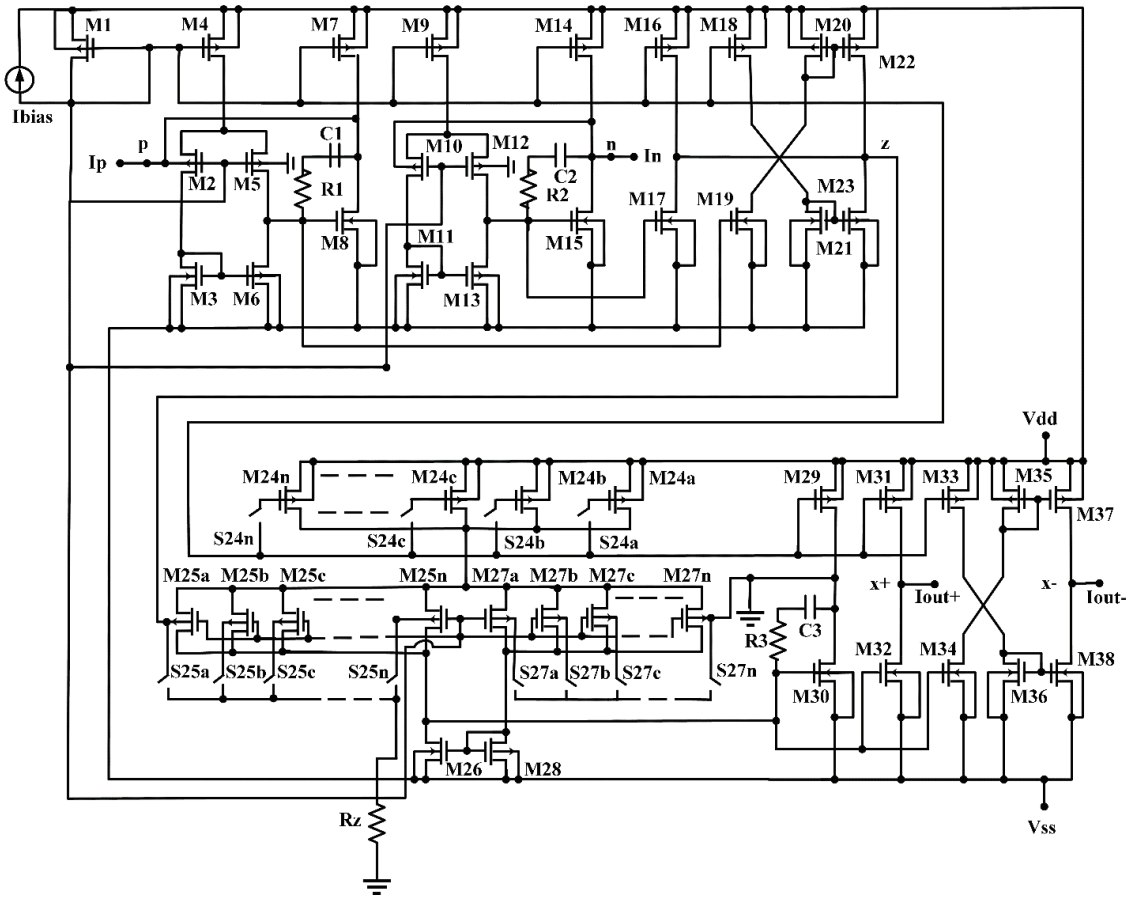

Figure 4. Transistor level implementation of proposed BDCDTA.

where V_{SG} is the source to gate potential, V_{TP0} is threshold voltage without any substrate voltage, μ_p is hole mobility for PMOS, C_{ox} is oxide capacitance and W/L is the transistor's aspect ratio. It shows that raising the aspect ratio can improve the total current I_D even when the gate to source and bulk to source potentials are unchanged.

The transistor-level implementation using this split transistor network in OTA_3 is proposed in Figure 4. We arranged transistors M25, M27 as well as M24 as a combination of 'n' parallel comparably small-sized transistors, as indicated by M25a to M25n, M27a to M27n, and M24a to M24n, respectively. A proper size selection with an increasing value of 'n' leads to higher transconductance and bandwidth. Neither any passive resistor R nor any other external resistor R_{set} as in conventional BDCDTA is used in our design. Furthermore, a current I_{bias} is used to properly bias the circuit and give electronic tuning capabilities, as shown in Figure 4. Transistor M1 is biased in such a way that it not only gives additional biasing current to all of the transistors utilized for this purpose but also provides sufficient potential to the gate terminal of the bulk-driven transistors of all three OTAs. Switches S25a to S25n, S27a to S27n, and S24a to S24n are used to select the required number of transistors as per the requirement of gain and bandwidth.

Small Signal Analysis of Proposed BDCDTA

Figure 5 shows the small signal equivalent circuit for OTA_3 of the proposed BDCDTA circuit for the i_{out+} section. Equations (5), (8), and (10) express the results obtained for v_{d27}, v_{d25}, and i_{out+}.

First, v_{d27} is evaluated from the right hand side of Figure 5 as-

$$v_{d27} = \left(\frac{-v_z}{2}\right)(g_{mb27a} + \cdots + g_{mb27n})(r_{o27a} \parallel \quad \ldots r_{o27n} \parallel r_{o28} \parallel \frac{1}{g_{m28}}) \quad (4)$$

Since $r_{o27a} \parallel \cdots r_{o27n} \parallel r_{o28}$ is having much higher value than $1/g_{m28}$, so equation (4) reduces to-

$$v_{d27} = \left(\frac{g_{mb27a} + \ldots + g_{mb27n}}{g_{m28}}\right)\left(\frac{-v_z}{2}\right) \quad (5)$$

Similarly, the left loop in Figure 5 gives the value of v_{d25} as-

$$v_{d25} = \left\{(g_{mb25a} + \cdots + g_{mb25n})\left(\frac{v_z}{2}\right) - g_{m26}v_{d27}\right\}(r_{o25a} \parallel \cdots r_{o25n} \parallel r_{o26}) \quad (6)$$

On putting the value of potential v_{d27} from equation (5) in equation (6) and also since the transistors M_{26} and M_{28} are identical (i.e. $g_{m26} = g_{m28}$), the following relation is obtained-

$$v_{d25} = \{(g_{mb25a} + \cdots + g_{mb25n}) + (g_{m27a} + \cdots + g_{m27n})\} \left(\frac{v_z}{2}\right)(r_{o25a} \parallel \cdots r_{o25n} \parallel r_{o26}) \quad (7)$$

Further, since all the transistors in sections M_{25a} to M_{25n} and M_{27a} to M_{27n} are identical, we can represent $g_{mb25a} = g_{mb25b} = g_{mb25n} = g_{mb27a} = g_{mb27b} = g_{mb27n} = g_{mb}$. It reduces equation (7) as-

$$v_{d25} = 2\,n\,g_{mb}\left(\frac{v_z}{2}\right)(r_{o25a} \parallel \cdots r_{o25n} \parallel r_{o26}) \quad (8)$$

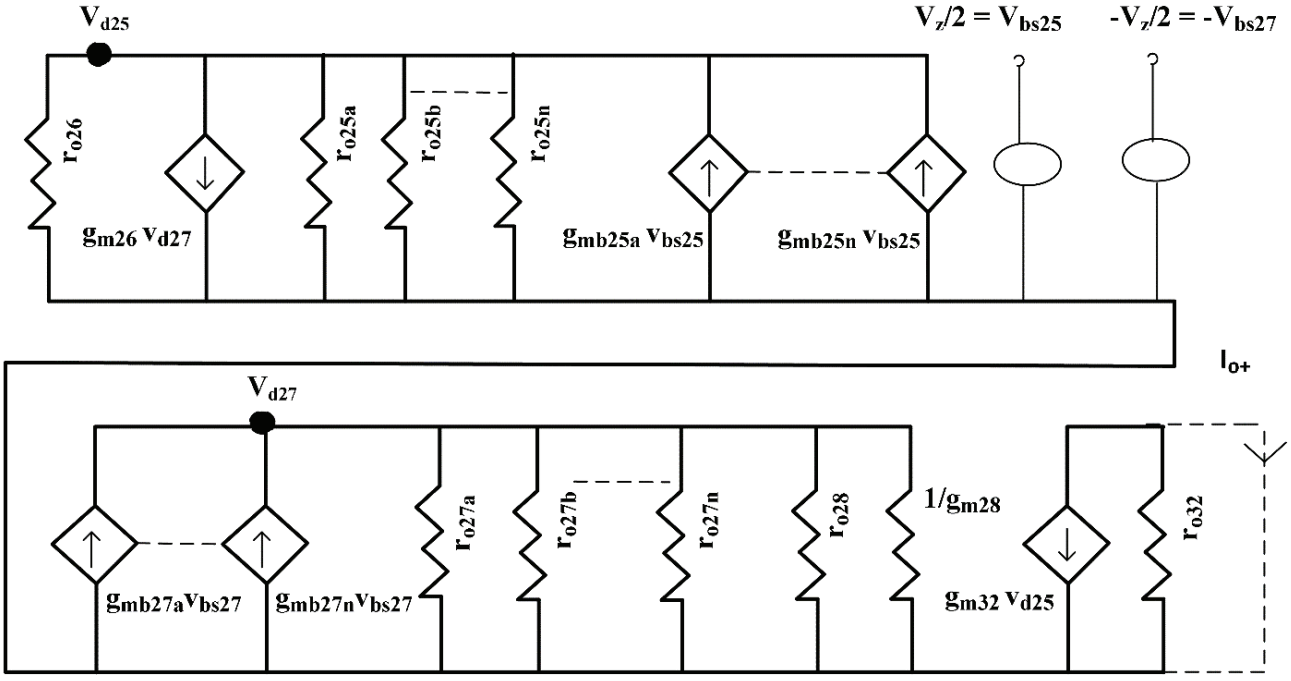

Figure 5. Small signal equivalent circuit for OTA3 of the proposed BDCDTA circuit.

Now, the output current i_{out+} from Figure 5 is obtained as-

$$i_{out+} = g_{m32}\, v_{d25} \quad (9)$$

On putting the value of v_{d25} from equation (8), and setting the transconductance g_{m32} such that $1/g_{m32} \approx (r_{o25a} \parallel \cdots r_{o25n} \parallel r_{o26})$, the value of i_{out+} is finally obtained as-

$$i_{out+} \approx n\, g_{mb}\, v_z \quad (10)$$

It implies that the output current is boosted by a factor of 'n', or the number of parallel transistors utilized in the OTA_3 section.

Analysis of Non-Ideal Characteristics

The schematic block design of the performance enhanced BDCDTA illustrated in Figure 2 is reconstructed in Figure 6, including the parasitic resistances of the input and output terminals of all OTA. All these resistances which are represented as R_{xa} to R_{xf}, appear at the input and output terminals of the OTA1, 2, and 3 as shown in Figure 6.

The current I_p coming out from the 'z-' terminal of OTA_1 and the current I_n moving towards the 'z_{+b}' terminal of OTA_2 can be expressed as follows-

$$i_p \approx (g_{mbOTA1z+} + 1/R_{xa})(-v_{xOTA1}) + \Delta I_{xOTA1} \quad (11)$$

$$I_n \approx (g_{mbOTA2z+a} + 1/R_{xb})(v_{xOTA2}) + \Delta I_{xOTA2} \quad (12)$$

Here, ΔI_{xOTA1} and ΔI_{xOTA2} are included as the offset currents because of the offset parameters of OTA1 and 2.

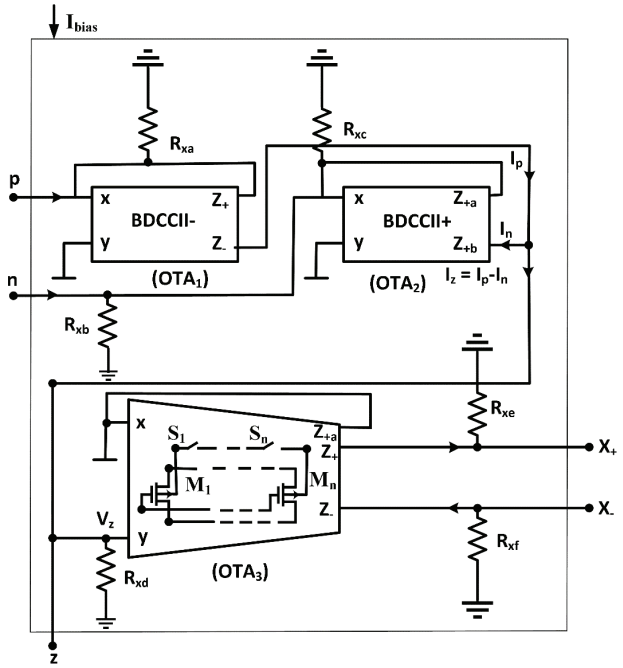

Figure 6. Schematic block diagram of proposed BDCDTA for non-ideal analysis.

Equations (11) and (12) indicate that the net value of the two OTAs current I_p and I_n increased from their ideal values by a factor of $1/R_x$ at the terminal and the offset current of the OTA. The lower the value of parasitic resistance R_{xa} and R_{xb}, the higher the value of these currents, however, if these values are sufficiently higher then equations (11) and (12) reduce to their ideal form with a value as $g_{mb}\, v_x$.

The output current at the intermediate terminal 'z' which is ideally the difference between these two currents I_p and I_n can now be expressed as follows-

$$I_z = \alpha_p I_p - \alpha_n I_n + \Delta I_z \quad (13)$$

where α_p and α_n are the current transfer ratios and Δ Iz is the offset current at the 'z' terminal whose values are expressed in equations (14), (15), and (16)-

$$\alpha_p = \left(\frac{R_{xd}}{R_z+R_{xd}}\right).\left(\frac{g_{mOTA1z-}}{g_{mOTA1z+}+\frac{1}{R_{xa}}}\right) \quad (14)$$

$$\alpha_n = \left(\frac{R_{xd}}{R_z+R_{xd}}\right).\left(\frac{g_{mOTA2z+a}}{g_{mOTA2z+b}+\frac{1}{R_{xb}}}\right) \quad (15)$$

$$\Delta I_z = \{g_{mOTA1z-}(\Delta v_{OTA1z+} - \Delta v_{OTA1z-}) + g_{mOTA2z+b}(\Delta v_{OTA2z+b} - \Delta v_{OTA2z+a})\}\left(\frac{R_{xd}}{R_z+R_{xd}}\right) \quad (16)$$

where Δv_{OTA1z+}, Δv_{OTA1z-}, $\Delta v_{OTA2z+a}$, and $\Delta v_{OTA2z+b}$ are all offset voltages of the two OTAs 1 and 2. For the ideal case resistances R_{xa}, R_{xb}, and R_{xd} are very high and the transconductance at the two output terminals of each OTA is the same. So, equations (14) and (15) reduce to $\alpha_p = \alpha_n = 1$.

Now the output current at the 'x_+' and 'x_-' terminal can be written from equation (10) as $i_{out\pm} = n\, g_{mb} \pm v_z$. Including the parasitic resistances R_{xe} and R_{xf} and the offset voltages at the 'z' terminal, the output current equation is derived as follows:

$$I_{x+} = n\, g_{mbOTA3}[v_z + (\Delta v_{z+} - \Delta v_{z+a})]\left(\frac{R_{xe}}{R_{x+}+R_{xe}}\right) \quad (17)$$

$$I_{x-} = n\, g_{mbOTA3}[v_z + (\Delta v_{z-} - \Delta v_{z+a})]\left(\frac{R_{xf}}{R_{x-}+R_{xf}}\right) \quad (18)$$

with the ideal conditions of offset voltages equal to zero and the parasitic resistances R_{xe} and R_{xf} values much higher than R_{x+} and R_{x-}, the output current equation reduces to the same value as in equation (10).

SIMULATION RESULTS, DISCUSSION, AND FUNCTIONALITY COMPARISON

The simulations were performed by using PSPICE CMOS 0.18 μm technology parameters. Supply voltages are taken as $V_{DD} = -V_{SS} = 0.5$ V and the biasing current I_{bias} is fixed at 5 μA. The resistance R_z at the z terminal is set to 5 kΩ to convert the input current difference to the

Table 1. CMOS transistor W/L ratios used in Figure 4

Transistors	W/L ratio (μm)
M 1	1.08/0.18
M 4, 9, 24	0.9/0.18
M 2, 5, 10, 12, 25, 27	0.9/0.18
M 3, 6, 11, 13, 26, 28	0.36/0.18
M 7, 14, 29	3.6/0.18
M 16, 18, 20, 22, 31, 33, 35, 37	3.96/0.18
M 8, 15	1.08/0.18
M 17, 30, 32	1.17/0.18

corresponding voltage. To separate the parasitic poles of the OTAs and make the first stage pole dominant, the resistance and capacitance combination utilized for frequency adjustment are 2.2 kΩ and 0.1 pF for each OTA stage. The transistors' W/L ratios used in the design as shown in Figure 4 are provided in Table 1.

Figure 7 shows the variation in output current as the number of transistors in the OTA_3 split network rises. It is important to note that as the number of transistors increases, so does the current amount and frequency range. The aspect ratios are adjusted so that when only single switches S_{25a}, S_{27a}, and S_{24a} are selected, the current received at the output terminal equals the difference between the two input currents I_p and I_n. The current increases by selecting the number of transistors with the help of switches S_{25a} to S_{25n}, S_{27a} to S_{27n}, and S_{24a} to S_{24n}. For a total of 6 transistors selected in the network, the output current value increases up to 4.9 mA as mentioned in Table 2. A comparison of the stated circuit's output current to the conventional one is additionally displayed in Figure 7, demonstrating that the conventional CDTA can only have an output current equal

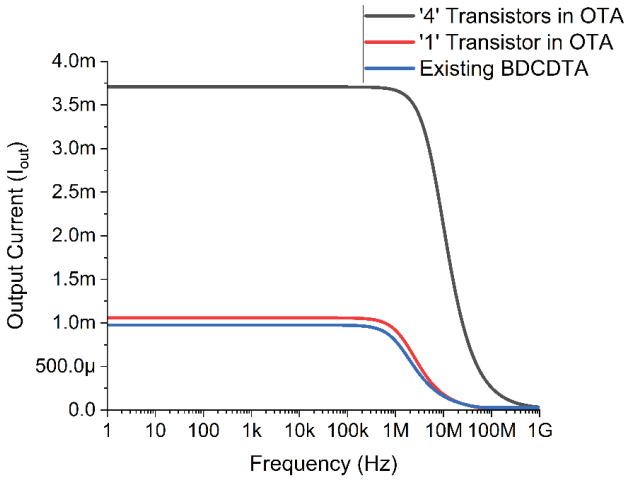

Figure 7. Variation of output current with increasing no. of transistors in OTA_3 network.

to the difference between the two input currents, with no further increase feasible. As a result, the proposed circuit can provide variable and increased output current depending on the requirements.

The DC transfer characteristics I_z/I_p and I_z/I_n for the current difference unit section of the proposed BDCDTA are similar to the conventional one, indicating that the linear operation range of input current I_p and I_n is up to -9 μA.

Figures 8 (a) and (b) depict the frequency response of the small-signal current gains I_z/I_p and I_z/I_n, respectively. The simulated value for I_z/I_p is 0.991 with a 3-dB bandwidth of 725 MHz, while the value for I_z/I_n is 1.044 with a 3-dB bandwidth of 2.94 GHz. The conventional circuit's simulated waveform displays similar gains but a substantially lower 3-dB bandwidth, namely 16.2 MHz for I_z/I_p and 51.6 MHz for I_z/I_n. As a result, the suggested circuit is capable

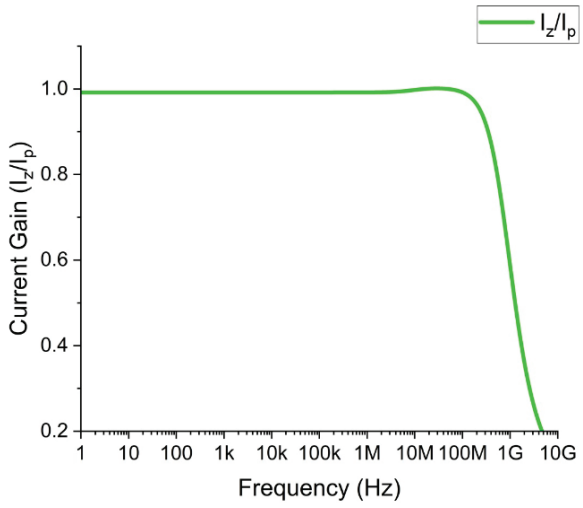

Figure 8(a). Current gain I_z/I_p

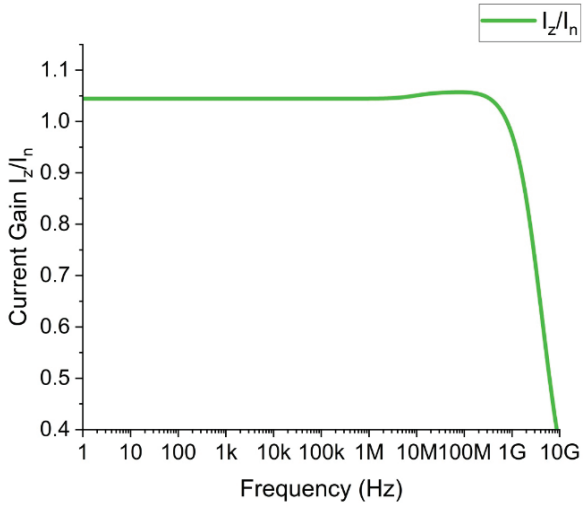

Figure 8**(b).** Current gain I_z/I_n

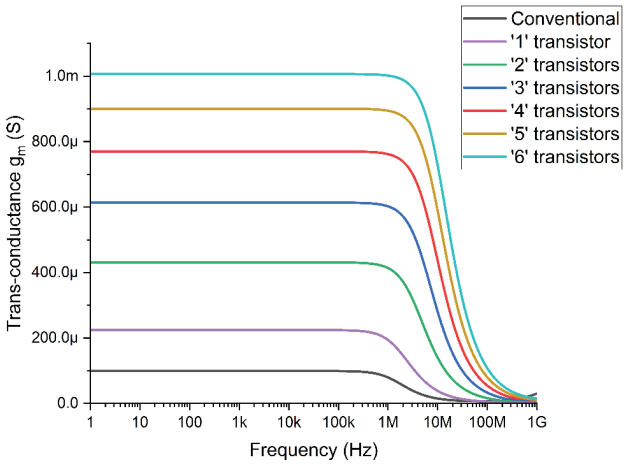

Figure 9. Transconductance waveform with increasing no. of transistors in OTA_3 network.

of providing current gains across a much wider frequency range.

Figure 9 shows a plot of OTA3's transconductance (g_m) versus the voltage V_z at its input terminal. Figure 9 also illustrates the standard circuit response, which has a fixed value of 99.12 µS for gm due to the R_{set} connection between the output and input terminals. Changing the value of R_{set} changes the g_m value up to a certain limit only and its frequency range is also limited. Using a single transistor in the split network results in a significantly higher gm value of 224 µS compared to the standard. The g_m value increases from 224 µS to 1 mS as the network's transistor count increases, outperforming the existing BDCDTA block in the literature.

Table 2 lists the parameters of the proposed BDCDTA circuit and compares its performance to the only existing BDCDTA [26] in the literature. The transistor count in the

Table 2. Parameter values and performance comparison to the only known equivalent work [26], as reported in the literature

Parameter	Reference [26] simulated at 180 nm	Proposed design (with '1' transistor in OTA3)	Proposed design (with '4' transistors in OTA3)	Proposed design (with '6' transistors in OTA3)
Supply voltage (V)	0.6	0.5	0.5	0.5
Power consumption (µW)	144.1	93.5	122.1	143.1
Bandwidth of I_z/I_p (MHz)	16.2	725	725	725
Bandwidth of I_z/I_n (MHz)	51.6	2940	2940	2940
DC current swing of I_p, I_n (µA)	-9	-9	-9	-9
Current gain (I_z/I_p)	0.992	0.992	0.992	0.992
Current gain (I_z/I_n)	0.999	1.0445	1.0445	1.0445
Output current (i_{out-}) (i_{in}=1 mA) (mA)	0.97	1.05	3.52	4.52
Output current (i_{out+}) (i_{in}=1 mA) (mA)	0.98	1.06	3.71	4.89
Transconductance (g_{mb}) (µS)	99.1	224.18	769.9	1006.4
Bandwidth of g_{mb} (MHz)	1.33	1.72	6.84	10.45

Table 3. Parameter values and performance comparison with other CDTAs

Parameter	Proposed design	Reference [26]	Reference [2]	Reference [3]	Reference [5]	Reference [7]	Reference [8]
		2011	2006	2021	2021	2022	2018
Device used	BDCDTA	BDCDTA	CDTA	CDTA	CDTA	FGCDTA	FGCDTA
Driving method	Bulk-driven	Bulk-driven	Gate-driven	Gate-driven	Gate-driven	Floating-gate	Floating-gate
Technology (µm)	0.18	0.18	0.5	0.18	0.18	0.13	0.18
Supply voltage (V)	0.5	0.6	2.5	0.9	1.5	1.4	1
Power Consumption (µW)	143.1	144.1	2190	432	525	2600	1100
Bandwidth of I_z/I_p (MHz)	725	16.2	104	475	0.45	2010	52
Bandwidth of I_z/I_n (MHz)	2940	51.6	55	480	0.45	1770	32
DC current swing of I_p, I_n (µA)	-9	-9	-78	-100	-100	-130	-75
Transconductance (µS)	1006.4	99.1	480	6000	--	6210	--

OTA of the proposed design varies from one to six. Table 2 shows that the transconductance has increased significantly by using this split transistor network technique. By suitably choosing the transistor sizes of the split network of OTA_3, the power dissipation is reduced, and bandwidth increases. The DC swing and linearity range are kept identical to the conventional design.

Compared to the conventional OTA network circuit, the suggested one transistor reduces power dissipation by 34.6%, while transconductance improves by 126% and BW increases by 29.3%. Furthermore, comparing the proposed six transistors in the OTA network circuit to the conventional one reveals that power dissipation is still reduced slightly by 0.69%, while transconductance improvement is 915.5%, BW enhancement is 685.5%, which is significantly higher than the conventional one, and it proves the usefulness of this proposed circuit.

Further, Table 3 lists some additional properties of the proposed BDCDTA circuit and compares its performance to other types of CDTAs available in the literature. It comprises the traditional CDTA, the BDCDTA, and the floating gate-based CDTA (FGCDTA). The suggested design's OTA has a total of six transistors. Table 3 indicates that the proposed BDCDTA has a substantially lower operating voltage than all existing types of CDTAs, as well as a correspondingly low power consumption. The suggested BDCDTA transconductance has increased significantly when compared to previously published BDCDTAs and conventional CDTAs, although it remains significantly lower than other gate-driven MOS-based CDTAs. The bandwidth achieved at the intermediate terminal I_z is also substantially higher than all others, but as expected, the DC current swing of traditional CDTA is much higher than that of the proposed CDTA.

It is clear from Table 3 that the proposed BDCDTA consumes much less power in comparison to all other existing CDTA and is capable of working at a lower operating voltage with higher bandwidth.

APPLICATION OF PROPOSED BDCDTA IN KHN BIQUAD FILTER

KHN Biquad Filter Using Proposed BDCDTA

The Kerwin-Huelsman-Newcomb (KHN) biquad filter structure can generate all three primary filter transfer functions: high-pass (HP), band-pass (BP), and low-pass (LP). KHN filter as reported in [2] is implemented here by using the proposed circuit as shown in Figure 10. Two blocks of the proposed BDCDTA circuit with two grounded capacitors are included in this circuit to implement the required functions and no other external component is used. Due to the grounded capacitance and fewer passive components, it is appropriate for the fabrication of integrated circuits (ICs).

The following transfer functions are found for the KHN filter –

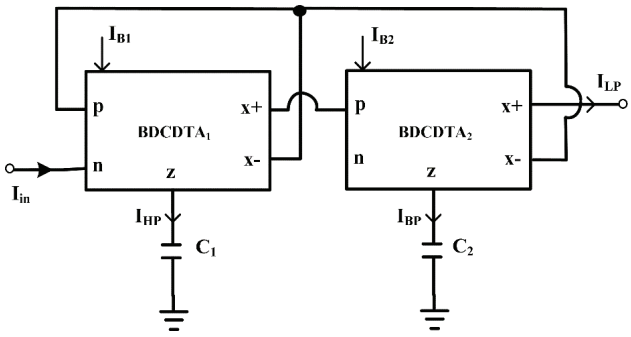

Figure 10. BDCDTA based current mode KHN biquad filter.

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2+(\frac{g_{mb1}}{C_1})s+(\frac{g_{mb1}g_{mb2}}{C_1C_2})} \tag{19}$$

$$\frac{I_{BP}}{I_{in}} = \frac{(\frac{g_{mb1}}{C_1})s}{s^2+(\frac{g_{mb1}}{C_1})s+(\frac{g_{mb1}g_{mb2}}{C_1C_2})} \tag{20}$$

$$\frac{I_{LP}}{I_{in}} = \frac{\frac{g_{mb1}g_{mb2}}{C_1C_2}}{s^2+(\frac{g_{mb1}}{C_1})s+(\frac{g_{mb1}g_{mb2}}{C_1C_2})} \tag{21}$$

where g_{mb1} and g_{mb2} are the transconductance gains of the proposed BDCDTA block. The important parameters frequency w_o and the quality factor Q of this filter are found as:

$$w_0 = \sqrt{\frac{g_{mb1}g_{mb2}}{C_1C_2}}, Q = \sqrt{\frac{g_{mb2}C_1}{g_{m1}C_2}} \tag{22}$$

To simplify the design, both C_1 and C_2 can be maintained the same, and the two identical blocks can be used to provide the same transconductance value, i.e., $g_{mb1} = g_{mb2} = g_{mb}$. This yields the expression for frequency as $w_0 = g_{mb}/C$ with a Q factor of 1.

Simulation Results of Biquad Filter Using Proposed BDCDTA

The PSPICE simulations were carried out to acquire a band-pass response with a center frequency of 1 kHz. The circuit parameters' design values are selected as follows: $C_1 = C_2 = 100$ nF while all the transistors aspect ratios are kept the same as mentioned in Table 1. The biasing current Ibias is set to 4 μA, and the resistance at the 'z' terminal R_z is 2.5 kΩ. The BDCDTA's OTA_3 section includes four transistors providing a transconductance gain of 685 μS.

Figure 11 shows the responses of the simulated KHN filter. The center frequency obtained as 1.08 kHz is in close approximation to the theoretically calculated value of 1.02 kHz. Furthermore, changing the number of transistors in the OTA_3 network alters the g_{mb} value, enabling this circuit to easily provide a shifted response with a flexible frequency range.

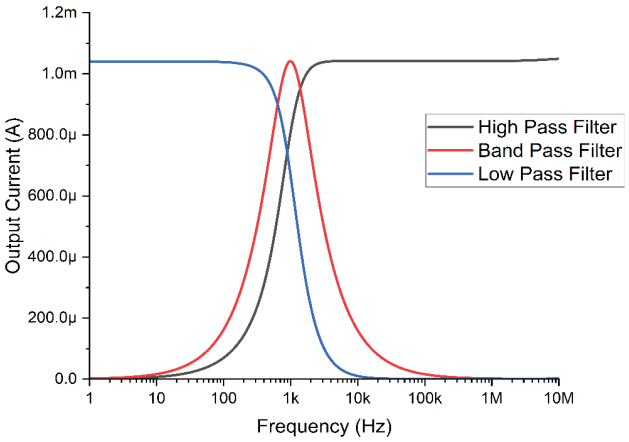

Figure 11. KHN biquad filter with BPF center frequency 1 kHz.

APPLICATION OF PROPOSED BDCDTA IN FREQUENCY AGILE FILTER

Frequency Agile Filter Using Proposed BDCDTA

The design of the BDCDTA has been validated once again by using a frequency agile filter structure. In communication systems, it is sometimes necessary to modify the tuning range at the receiving end. Frequency agile band-pass filters with changeable bandwidth are important for this application. The idea of agile filters was initiated in [10], which shows its implementation based on a second-order filter block having both band pass [24, 25] and low pass output functions. Designs for implementing frequency agile filters utilizing CDTA were proposed in [11, 12], however, the proposed new frequency agile filters based on BDCDTA will function with significantly lower power consumption and will also consume much less area in comparison to the previous designs.

This study also suggests a modified strategy for reducing the overall area. The proposed current-mode frequency agile filter based on our performance-enhanced BDCDTA is shown in Figure 12. For the second-order filter, we have taken our designed KHN biquad filter as shown in Figure 10. The modification is carried out such that instead of using a few transconductance amplifiers in the feedback section, only one BDCDTA block with a variable gain is utilized. It reduces the overall count of BDCDTA utilized, and thus the circuit complexity.

According to equations (20), (22), and Figure 12, by routine analysis, it is easy to get the circuit's transfer function as:

$$\frac{I_{BP}}{I_{in}} = \frac{\frac{g_{mb1}\,s}{C_1\left(1+g_{mbfb}.R_Z\right)}}{s^2+\frac{g_{mb1}\,s}{C_1\left(1+g_{mbfb}.R_{Z3}\right)}+\frac{g_{mb1}g_{mb2}}{C_1C_2\left(1+g_{mbfb}.R_{Z3}\right)}} \quad (23)$$

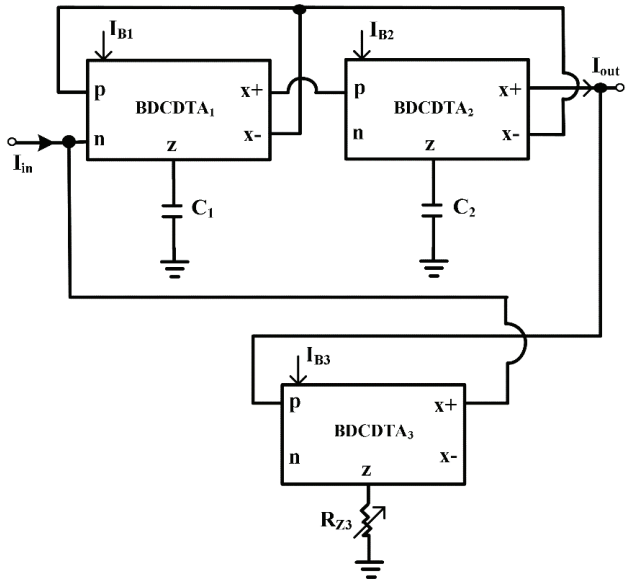

Figure 12. Current mode frequency agile filter based on proposed BDCDTA.

$$\text{with } w_0 = \sqrt{\frac{g_{mb1}g_{mb2}\left(1+g_{mbfb}.R_{Z3}\right)}{C_1C_2}}, \text{ and}$$

$$Q = \sqrt{\frac{g_{mb2}C_1\left(1+g_{mbfb}.R_{Z3}\right)}{g_{mb1}C_2}} \quad (24)$$

From the above equations, it is easy to investigate that the characteristic parameters of the agile filter i.e., center frequency, Q-factor, and gain, are dependent on the feedback amplifier's transconductance and the external resistance R_z connected to its 'z' terminal. Instead of using multiple feedback amplifiers, we employed a single amplifier in the feedback section with varying R_z to achieve the desired results. In this manner, the proposed circuit contains a simple structure with minimal active and passive components.

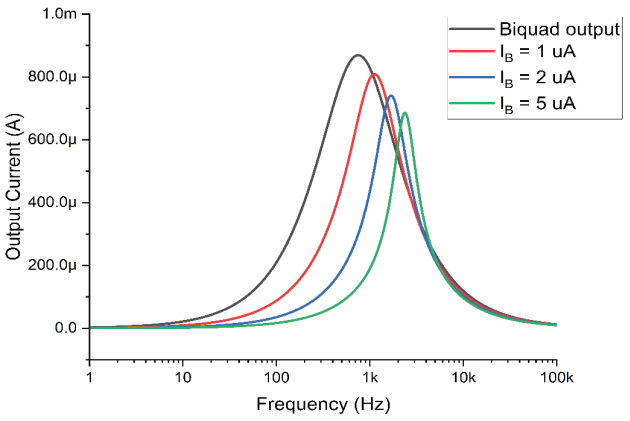

Figure 13. Simulated waveforms of the current mode frequency agile filter.

Simulation Results of Frequency Agile Filter Using Proposed BDCDTA

To simulate the circuit as in Figure 12, the biasing current in the second order section was kept at 2 μA with other parameters of this section same as in the KHN filter. The initial biasing current and R_z values in the feedback amplifier were set to 1 μA and 2.5 kΩ, respectively. The resulting waveform shows a shift in the center frequency of the bandpass filter from 750 Hz to 1 kHz as shown in Figure 13. The biasing current of the feedback amplifier section was changed from 1 μA to 2 μA and then to 5 μA with R_z from 2.5 kΩ to 5 kΩ and then 10 kΩ and corresponding center frequency shifted waveforms were obtained from 1 kHz to 1.6 kHz and then 2.2 kHz. The simulated results are very close to the calculated theoretical values of 0.9, 1.3, and 2 kHz.

CONCLUSION

The simulation results for the proposed BDCDTA design indicate significant improvements in both transconductance and bandwidth. The power dissipation is also less in comparison to the existing circuit even increasing the number of transistors in the split network. The biquad filter works well with a center frequency of 1 kHz; however, it may be easily adjusted to any other value required using passive components. The frequency-agile filter application proves its usefulness in communication systems with low power consumption.

This BDCDTA can be used for a variety of applications, particularly when a range is required because it is simple to alter the amount of transistors in the OTA's split network using switches or it can simply be done by varying the input bias current. This circuit is appropriate for applications with low operating voltages; however, if the operating voltage is high, standard CDTA can be used because this design uses a bulk-driven method and so cannot function at higher voltages. Due to bulk-driven limitations, very high bandwidth, such as GHz or THz, is also not achievable. However, due to its high gain and low power consumption, the proposed design is expected to be useful not only in biomedical instruments but also in a wider range of applications.

AUTHORSHIP CONTRIBUTIONS

Authors equally contributed to this work.

DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

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