Sigma Journal of Engineering and Natural Sciences
Web page info: https://sigma.yildiz.edu.tr
DOI: 10.14744/sigma.2025.00120

Research Article

Enhanced content-addressable memory with ternary content-addressable neural network-based auto encoder

P. Prabhu THAPASWINI[1,*]

[1]*Department of Electronics and Communication Engineering, Sri Padmavati Mahila University, Tirupati, 517502, India*

ARTICLE INFO

Article history
Received: 01 February 2024
Revised: 15 March 2024
Accepted: 08 August 2024

Keywords:
Deep Convolutional Neural Network, Embedded and Expandable Ternary Content Addressable Memory, Static Random-Access Memory and Field Programmable Gate Array, Ternary Content Addressable Memory

ABSTRACT

In digital electronic devices, the IC3-FPGA circuit plays a significant role in various applications in the networking, medical, and communication sectors. Fundamentally, TCAM is the chef component in the circuit responsible for the searching and pattern-matching operations. The error in the TCAM disturbs the overall functions of the IC3-FPGA circuit, such as addressing errors, data corruption, addressing errors, and much more. Besides, TCAM errors lead to hardware failure in the networking systems. Therefore, it is essential to correct the TCAM errors in order to improve the system›s efficiency. To attain this, traditional researchers attempted to accomplish efficient TCAM correction but lacked efficiency. To resolve the problem, the proposed system employs ADCNN (Enhanced Content-Addressable Deep Convolutional Neural Network) to enhance the efficiency of the TCAM (Ternary Content-Addressable Memory) correction system. The CNN is utilized for the capability of translation variance, localized weight sharing, etc.; however, it lacks long-term dependencies. To resolve the issue, the presented model incorporated a genetic algorithm for the weight-based fitness value in the ADCNN. Correspondingly, the input of the respective research is the gate level inputs, where the outcome is the error-corrected TCAM. The performance of the TCAM is evaluated using performance metrics such as area, delay, and power. Moreover, a comparative analysis of the presented system with the classical model is processed to expose the efficiency of the proposed method. The respective research is intended to contribute to the research related to the improvement of the TCAM system.

Cite this article as: Thapaswini PP. Enhanced content-addressable memory with ternary content-addressable neural network-based auto encoder. Sigma J Eng Nat Sci 2025;43(4):1276–1289.

INTRODUCTION

The IC3-FPGA chip is a certain kind of FPGA circuit utilized for various applications such as IoT (Internet of Things), aerospace, networking, communications, etc. It comprises interconnects, logic blocks, and input and output interfaces. Consistently, TCAM (Ternary Content Addressable Memory) is the component in the circuit computer memory widely used by digital systems for high searching mechanisms [1, 2]. Particularly, EE-TCAM is the embedded and expandable function that delivers a way to arrange the usage of the TCAM memory in the design

*Corresponding author.
*E-mail address: thapaswiniputta.spmvv@gmail.com

This paper was recommended for publication in revised form by Editor-in-Chief Ahmet Selim Dalkilic

applications with effective lookup functions[3]. The error in the TCAM affects the performance of the networking devices by disturbing the overall functionality of searching and matching operations. The TCAM errors influence the IC3-FPGA circuit in various factors such as search accuracy, degradation of efficiency, data integrity, etc. Moreover, this error impacts the operation with unpredictable and improper pattern matching and searching outcomes, which lead to issues in the devices, such as security vulnerabilities, routing errors, and dropped packets. Therefore, it is significant to correct the TCAM errors in order to enhance the efficiency of the networking devices.

Correspondingly, several conventional models utilized diverse techniques for the enhancement of TCAM efficiency. For instance, in the traditional model, the TCAM-based framework utilizes a D-CAM block with 48 bytes TCAM in the 64-based lookup tables. The implementation of the conventional model has been processed with the size of 512 X 155 on Xilinx Virtex-6 FPGA. The outcome of the classical research represents better efficiency with a throughput value of 58.8% [4]. Congruently, power-aware-based RPE-TCAM-based architecture has been utilized in the existing mechanism. Besides, it permits a part of the hardware for the process of the search function in the system. Moreover, it has been used in broad space exploration for identifying the optimal amount of banks in the Xilinx FPGA. The experimental results illustrate better efficiency of the traditional model [5]. In the same way, an optimal weighted load balancing-based framework has been used in the classical method. Prefix matching TCAM rules are available for limiting the design in the expected partition. Besides, the algorithm has been implemented to identify a partition close to the expected one [6]. Correspondingly, ME-TCAM (magnet electric effect aided TCAM) has been designed for the enhancement of TCAM efficiency. Here, potential array level search and write efficiency has been used to evade large heating present in the magnetic devices.

The outcome of the stimulation signifies better performance [7]. Accordingly, numerous existing types of research utilized various techniques for TCAM performance enhancement. However, the error correction-based TCAM model is limited in the classical systems. Moreover, efficiency is lacking in the error correction TCAM-based traditional models.

To solve the problem, the proposed study used a specific set of procedures for the TCAM error correction enhancement efficiently. Predominantly, the Verilog function is used for the process of designing for correcting errors related to TCAM; thereby, the current model uses EE-TCAM. The sub-tables were processed for dividing and establishing memory of TCAM memory to the minor sub-tables. The memory division improved the memory resource utilization in TCAM from accessible memory storage. In a similar vein, SRAM cells in the TCAM stocks data, which is explored in the system. In the following, the data contained in the SRAM is encoded automatically with the method known as ADCNN (Enhanced Content- Addressable Deep Convolutional Neural Network) along with 16, 32, and n bits. Through this, a genetic algorithm is used for attaining weight related fitness value for the function of encoding. Moreover, the decoder layer processes the function of decoding that is related to correcting errors for SRAM bits. In conclusion, the proposed research performance is measured through power, delay, and area. The major contributions of the proposed system are represented in the following:

- To employ ADCNN for the error correction in TCAM-IC3 FPGA circuit to enhance the efficiency of the system performance.
- To evaluate the performance of the error correction with particular metrics such as area, power, and delay.
- To reveal the greater efficiency of the respective method, a comparative analysis is carried out with the proposed system with existing research.

Paper Organization

The paper is organized based on the effective techniques applied in enhancing the TCAM system by analyzing traditional models discussed in Section II. Section III indicates the technique of the proposed method. Further, the results accomplished by the respective method are depicted in Section IV. Finally, the conclusion with the future work of the respective model is signified in Section V.

REVIEW OF LITERATURE

The section represents the analysis of the various existing research in the detection and correction of TCAM.

In the conventional model, protection architecture has been designed for SRAM-aided TCAMs. To attain this, utilizes a single-bit parity technique that has been used for the detection of fault with the minimum critical path. Besides, binary-encoded TCAM has sustained SRAM-based TCAM to design low response time error correction. The outcome of the classical method signifies better efficiency [8]. Similarly, the detection and correction of errors in the TCAM are constructed using the traditional model. For that, per word, DMC is utilized to ensure the reliability of the memory. Besides, a protection code with a decimal algorithm is used to identify errors in the TCAM. The experimental results signify the classical method attained better efficiency in the protection level against larger MCUs [9]. Accordingly, the traditional method focused on implementing a low response time method in the SRAM-aided TCAM protection system [10]. Here, single-bit parity has been utilized for the detection of fault, and the upgraded binary encoded in the TCAM table is processed for low response time in the error correction. The experimental results signify better performance in the error correction and detection of TCAM [11]. Consistently, existing research implemented the correction of subtle errors in calculating data in TCAM. To accomplish this, N-SEARCH

KEY TCAM has been utilized in the conventional method where the ternary memory uses the particular LUT for the matching function. Moreover, the amount of improper segregation in the ratio of reduction with upsurge ratio in forbearance time and parameter has been used to identify and correct the errors. The outcome represents better efficiency with average time consumption and error identification [12].

Correspondingly, the ER-TCAM-based system has been used in the pioneering mechanism for attaining error-resistant possessions. Besides, single-bit parity with fault detection has been used with a slight critical path. Moreover, PMA has been designed in the classical system for the purpose of data transferring among chief memory to the devices. The stimulation outcome signifies better efficiency [13]. Likewise, LFSR based error detection has been built in the classical approach. Here, a low response time mechanism has been used for the LFSR-aided TCAM protection. Besides, the error correction system has been functioning in the lookup process in a recurrent manner. The stimulation outcome depicts better performance in the high search function and error correction in TCAM [14]. Similarly, binary encoded TCAM [15] aided table maintained SRAM for the upgrade mechanism for accomplishing low response time error correction. Moreover, SRAM aided TCAM [16] in the detection and correction of errors with the size of 1024 X 40. The better performance of the classical model has been verified over the results [17]. In the same way, the existing model designed an error resilience system in the LSFR-based TCAM for FPGA for the purpose of packet classification for open flow and SDN. It utilizes minimal overhead for enhancing the detection process where straightforward single bit parity has been deployed for fault detection. The simulation results represent better efficiency [18].

Similarly, a fault tolerance-based system has been constructed in the classical model for resolving failure or fault effects in the TCAM. For that, VLSI-aided architecture has been used for the simple XOR function in the significant bits. The outcome of stimulation represents better efficacy in the design of fault tolerance-aided TCAM [19]. Correspondingly, a soft error tolerance system has been built in the traditional mechanism through ML (Machine Learning) based techniques. Here, multiple-bit flip tolerant TCAM signifies the soft error problem with the X-keys. The techniques utilized in the conventional model are classified into two, such as, X-key matching and statistical training. Accordingly, statistical training has been used to define effective amounts in don't care where x-ray matching has been utilized to TCAM [20, 21] for correcting the bit flip errors. The experimental results represent better efficiency [22]. In the same way, numerous conventional techniques have been utilized in various strategies for the enhancement of TCAM for several applications [23]. However, error correction-based TCAM design is limited in the existing research. For instance, the design of TCAM on the basis of priority decision in the memory technology. For that, MNV-TCAM has been utilized in the traditional mechanism to achieve high reliable, high speed model [24]. Likewise, the design of error correction in the TCAM has been utilized in the parallel memory allocation through particular error-resilient properties. It has been intended to identify and correct errors in parallel data allocation. Besides, a priority circuit has been utilized to produce diverse levels of priorities with the data transfer among slave and master devices. The experimental outcome signifies better efficiency [25].

Problem Identification

The section represents the limitations identified in the analysis of existing research.

- Several conventional studies focused on enhancing TCAM in various dimensions. However, error correction-based TCAM is limited in traditional models [20, 21].
- Most of the classical methods centered on the detection of fault or error in TCAM, where correction of error or fault is inadequate in existing systems [18, 22].

PROPOSED METHODOLOGY

The TCAM errors influence the searching process in the IC3 FPGA system by disturbing the functionality and efficiency of the IC3-FPGA circuit. To resolve the problem, several models utilized various techniques but lacks in efficiency. To overcome the issue, the proposed system used ADCNN for error correction in TCAM. The figure.1 represents the design flow of the respective method.

Figure 1 signifies the methodological flow of the presented research. From the figure, it is identified that the projected system possesses a certain set of procedures for error correction in TCAM. Accordingly, the proposed system's input is the gate-level input, and the expected output is the error-corrected TCAM. Correspondingly, efficiency is calculated using performance metrics such as delay, power, and area.

Primarily, the Verilog function is initialized to design the error correction-based TCAM where the proposed model utilized EE-TCAM. The sub-tables are processed for establishing and dividing the memory of TCAM into the minor sub-tables. The division of the memory enhances the utilization of memory resources in TCAM from the obtainable memory space. Accordingly, SRAM cells in TCAM stocks data that is searched in the system. The data in the SRAM is auto-encoded with the technique called AE-DNN (Auto Encoder Deep Neural Network) with 16, 32, and n bits. From that, a genetic algorithm is utilized to obtain weight-based fitness values for the encoding function. Further, the decoder layer processes the decoding function, which is based on the error correction for the SRAM bit. Finally, the performance of the respective research is calculated using area, power, and delay. The detailed description

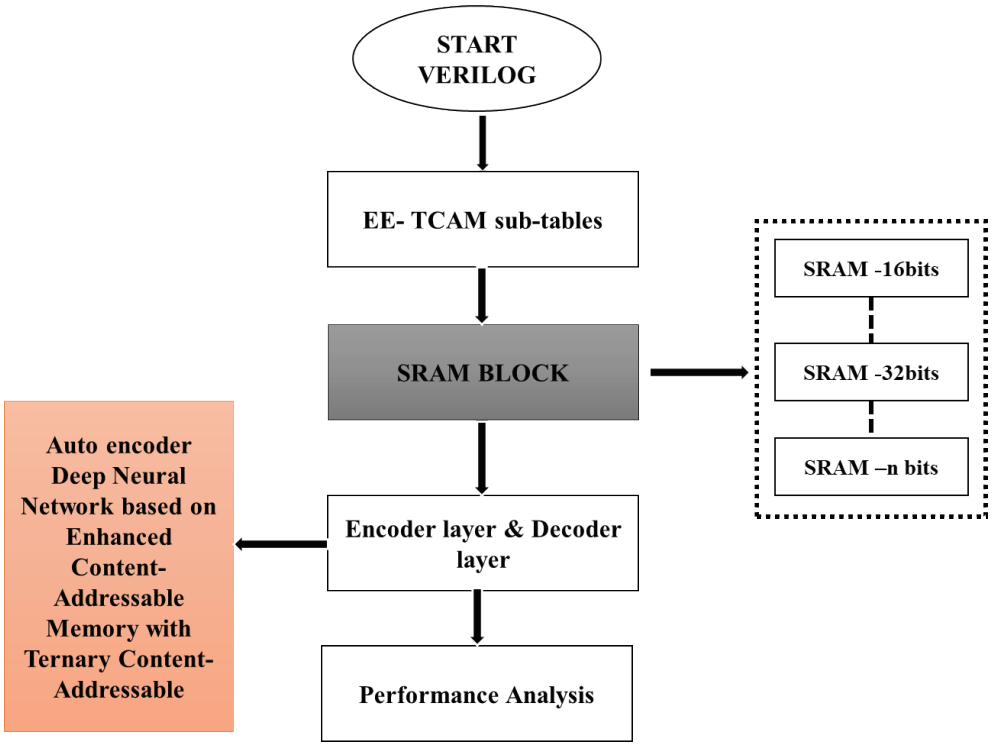

Figure 1. Design flow of the proposed model.

of the proposed techniques is deliberated in the following subsections:

EE-TCAM Sub-Tables

The EE-TCAM sub-tables are the particular mechanism of arranging and separating the memory into sub-tables. The division of the memory improves the utilization of data resources in TCAM from the memory space. Besides, it supports maintaining and assigning memory for certain requests. In the respective system, EE-TCAM sub-tables are embedded with the greater structure of TCAM, which enables better table lookups for packet forwarding and processing.

SRAM Block

The SRAM is the type of memory that stocks data in a manner of static state. It is used as the cache memory in the TCAM for a better search mechanism. Compatibly, TCAM utilizes the capabilities of SRAM and CAM for better speed searching functions and matching purposes, which are based on the memory cells in the system. Correspondingly, SRAM cells in the TCAM make effective searching with the particular type of content and pattern. The data in the SRAM is stocked in the size of 16 bits.

Encoder and Decoder Layer – Auto Encoder Deep Neural Network

In the respective method, data in the SRAM is processed with the auto encoder function with DNN based mechanism. For that purpose, genetic algorithm-based weight optimization is used in the presented model. The proposed model employs DNN based mechanism for the enhancement of the error correction in TCAM. The figure.2 represents the architecture of the projected approach.

Figure. 2 signifies the architecture of the presented method where DNN is used for the auto-encoder mechanism. This system comprises SRAM data with a low-dimensional depiction and a decoder network for rebuilding the original input data. The process of integrating the autoencoder with TCAM identifies the variance in the data, which is further corrected in the respective model. Therefore, DNN for the auto encoder that enhances anomaly detection in TCAM. Initially, DNN identifies an error in the SRAM block. Accordingly, encoding of data stocked in SRAM bit, which includes the addition of redundant bits to the original data for the process of error correction and detection. Here, a genetic algorithm is utilized for weight-based fitness value. Further, the allocation of supplementary memory in the SRAM bit stocks the redundant bits that are produced in the encoding mechanisms. Then, in the process of reading data from the SRAM bit, encoded data is recovered with the decoding mechanism.

Convolutional Neural Network

CNN is the type of artificial neural network for the detection and classification of particular features in the data. The advantages of using CNN are localized weight

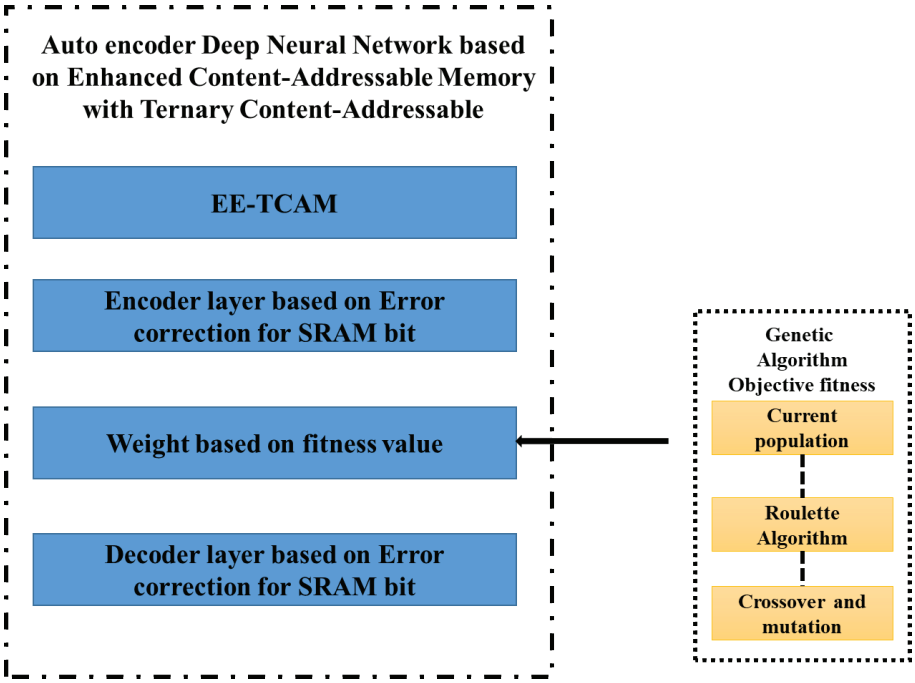

Figure 2. Architecture of proposed model.

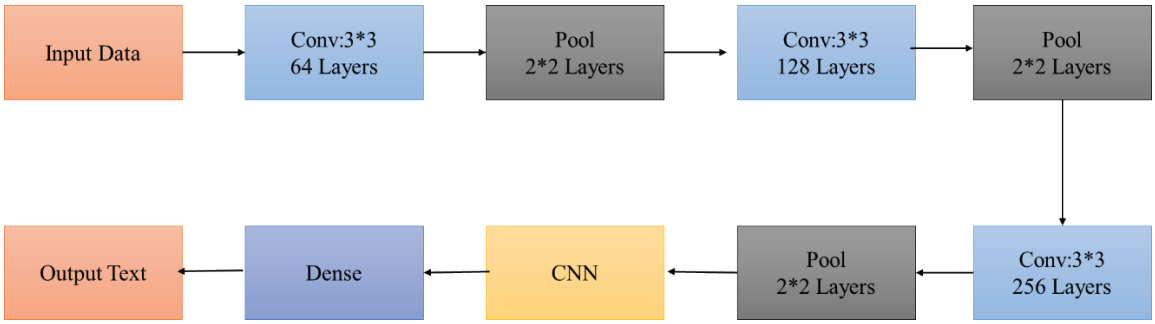

Figure 3. CNN architecture.

sharing, translation invariances, hierarchical feature learning, parallel processing, etc. The figure.3 represents CNN architecture.

The figure.3 signifies CNN architecture. The chief feature of CNN is the capability of automatically learning and taking related features from the input data with the convolution function. It comprises of learnable filters to the input data to identify specific patterns and features. Further, pooling and fully connected layers in the CNN enhance the detection performance. The pooling layers minimize the spatial dimension of the feature map, which supports extracting significant features in the data where fully connected layer process prediction with extracted features. The pseudo-code of CNN is signified in the pseudocode.1.

Correspondingly, CNN contains various advantages in the prediction mechanism, but it still comprises certain limitations, such as the incapability of taking long-term dependencies in the data. To overcome the limitations, DCNN is utilized in the respective research.

Deep Convolutional Neural Network

The DCNN is the variant of the CNN mechanism that overcomes the problem of apprehending long-term dependencies by using a dilated convolution function. It is the atrous convolution function that uses space among the kernel elements in the function of convolution. This process enhances the amount of parameters in the system. Correspondingly, forward propagation is utilized to generate a set of hidden units at the top of the convolutional layer. It is processed to define the activated unit for every epoch. The algorithm.1 signifies the process in the deep convolutional neural network.

Pseudo code.1. Convolutional Neural Network

Operation for CNN System
Code
Operation CNN_System (x_i)
Weights ← Determine Weights
Biases ← Determine Biases
X_i ← Reshape(X_i, shape ← {$Pixel_{X_i}$, $Pixel_{Y_i}$, $Slice_{Count}$}
conv1 ← Relu Activation Function (conv3D(x_i, Weights[0]) + biases[0])
conv1 ← Dropout(0.5)
conv1 ← Max_pool3D(conv1)
conv2 ← Relu Activation Function (conv1D(x_i, Weights[1]) + biases[1])
conv2 ← Dropout(0.5)
conv2 ← Max_pool3D(conv2)
Fully Connect ← Reshape(conv2 , InverseWeights[2])
Fully Connect ← Relu Activation Function (Fully Connect ∗ Weight[2] + Biases[2]
Fully Connect ← Dropout(0.8)
output ← Fully Connect ∗ Weights[3] + biases[3]
Return Outcome
End Operation

Algorithm.1.Deep Convolutional Neural Network

***Step*1**: *Gather data through* 4 *techniques as* $v_i \in \mathcal{R}_o\ M_o \times T_i$, M_o *as channel size*, T_i *as time samples*
***Step*2**: *Start CNN filter weight* $W_{ct_i}^{ik_o}$ ik *for* c_i *th* ($c_i = 1, 2, \ldots, M_o$ *represents Size of chaanel*) *channel*, t_i *th* ($t_i = 1, 2, \ldots, T_i'$ *depicts sizeof time sample*) *time sample*, k_i *th* ($k_i = 1, \ldots K_i$ *denites size of feature map*) *kernel, and* ii *th* ($ii = 1, \ldots N_i$ *mentions isze of convolutional layer*) *layer*.
***Step*3**: Start CNN fully connected weight U_{p_i}, q_i , where p_i signifies size of feature in the top convolutional layer, q_i is the hidden unit size, and j signifies size of fully − connected layers.
***Step*4**: *For* $ii < N_i$ (N_i *is the convolutional layer*)
***Step*5**: convolution $(v_i)k_iT_i = \text{ReLU} \sum_{c_i,t_i}^{M_o,T_i} W_{ct_i}^{ik_o}$
***Step*6**: v_{ii} ← convolution $(v_i)k_iT_i$
***Step*7** : v_{ii} ← pooling (v_i)
***Step* 8**: *Repeat level in* $ii = ii + 1$
***Step* 9**: *For* $jj < F_{ci}$ (F_{ci} *is the fully − connected layer*)
***Step* 10**: $v_i \leftarrow F_{ci}(v_i)$
***Step*10** Repeat level: j j ← j j + 1
***Step*11**Back − propagate Loss (v_i, L_i), L_i as the true label

Performance Analysis

The proposed model›s performance is calculated using the performance metrics to analyze the efficiency of error correction in terms of area, power, and delay.

RESULTS AND DISCUSSION

This section represents the outcome attained by the presented method, depicting EDA (Exploratory data analysis), performance metrics, performance analysis, and comparative analysis.

Exploratory Data Analysis

The EDA is used to view and analyze the input data. Figure 4 signifies the input and output of the presented model.

Figure 4 signifies the input and output of the respective research, where input is the gate-level input and outcome is the error-corrected TCAM.

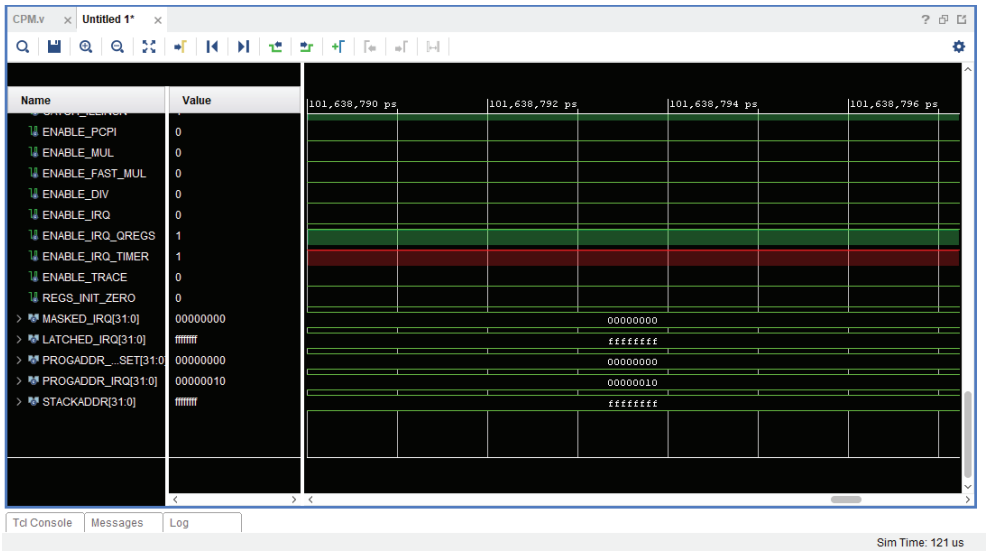

Figure 4. Input of the proposed method.

Tools and Requirements

This section deliberates the tools and required factors needed for the respective research in TCAM error correction.

Chip - IC3 FPGA

Tool - XILINX - VIVADO 2018.2

Performance Metrics

The section represents the performance metrics utilized to analyze the efficiency of the respective research.

1. **Area**
   The chief significant parameter of large parallel devices is an area that enhances the efficiency of the system. This inspires the technique to utilize several cryptographic implementations.
2. **Power**
   Encryption is deliberated as an essential part of the system that utilizes a certain volume of exceptional possessions like memory, CPU time, and battery power. The power is evaluated by computing the energy utilized per unit of time.
3. **Delay**
   A propagation delay is initiated when the key transported is late to receive. If the delay decreases, the system›s efficiency and optimization increase.

Experimental Results

This section depicts the outcome of the projected system. Figure 5 signifies the circuit layout of the presented system.

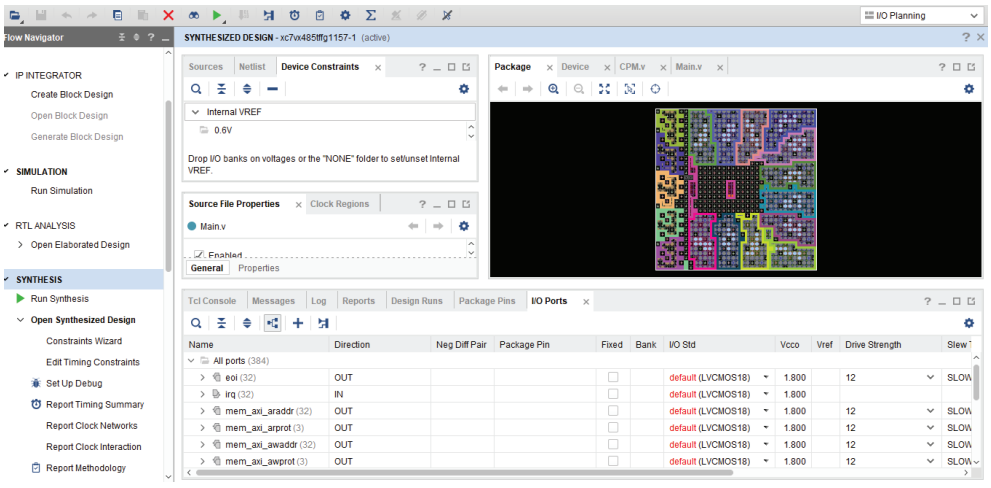

Figure 5. Circuit layout of the respective method.

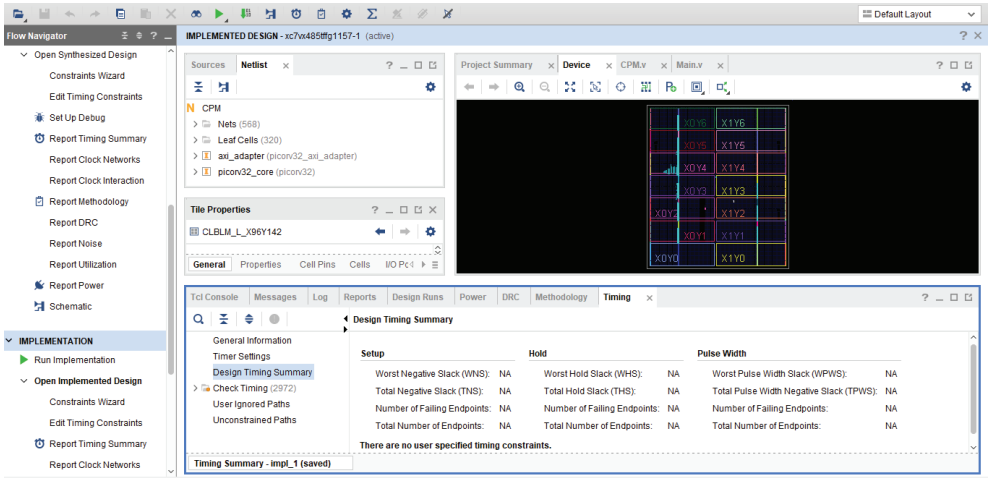

Figure 6. Circuit gates of the IC3 FPGA chip.

Figure. 5 depicts the circuit layout utilized in the proposed mechanism. It represents the IC3 FPGA chip utilized in the projected model for error correction TCAM. The figure.6 signifies the circuit gates used in the proposed approach.

Figure. 6 depicts the gates in the TCAM of the IC3 FPGA chip. The figure.7 signifies the circuit stimulation of the respective system.

Figure 7 illustrates the stimulation of the proposed method. Table 1 and Figure 8 represent the result of the proposed mechanism.

Figure 8 and Table 1 describe the result attained by the proposed mechanism in error correction in TCAM. The respective model attained an efficiency of 97%, which signifies greater efficacy. Here, power consumption is 31.06 w, revealing the proposed model's lower power consumption.

Table 1. Outcome of the respective method

S.no	Performance metric	Outcome
1.	Efficiency	97%
2.	Delay	3.066
3.	Area	4.156
4.	Power	31.605W

Comparative Analysis

The efficiency of the respective system is compared with the existing research to evaluate the performance. The outcome of the comparative analysis is signified in this section. Table 2 and Figure.9 signify the comparative analysis of the proposed model with the existing method.

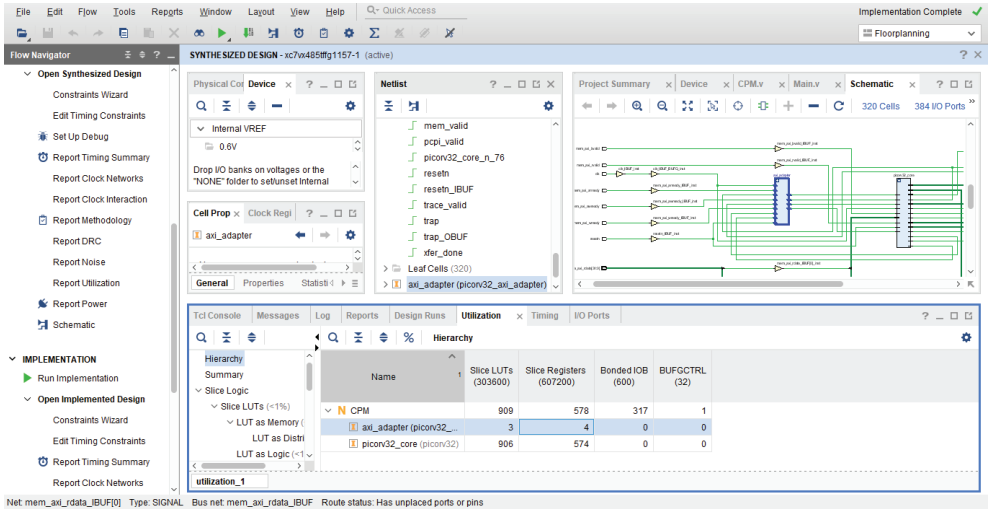

Figure 7. Circuit stimulation of the presented model.

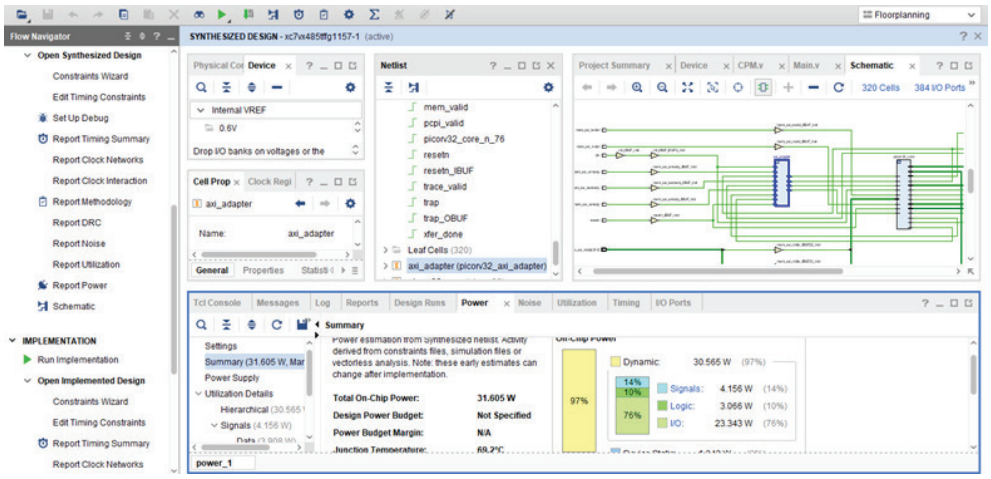

Figure 8. Outcome of the presented method.

Table 2. Comparative analysis of respective system with classical model

Method	Propagation delay (ns)	No of SLICES	Power consumption
CF	6.035	47	3.004
TBDD	5.048	197	5.87
PPRM	5.552	120	1.57
MPPRM	4.581	76	1.568
Proposed	**3.125**	**32**	**1.024**

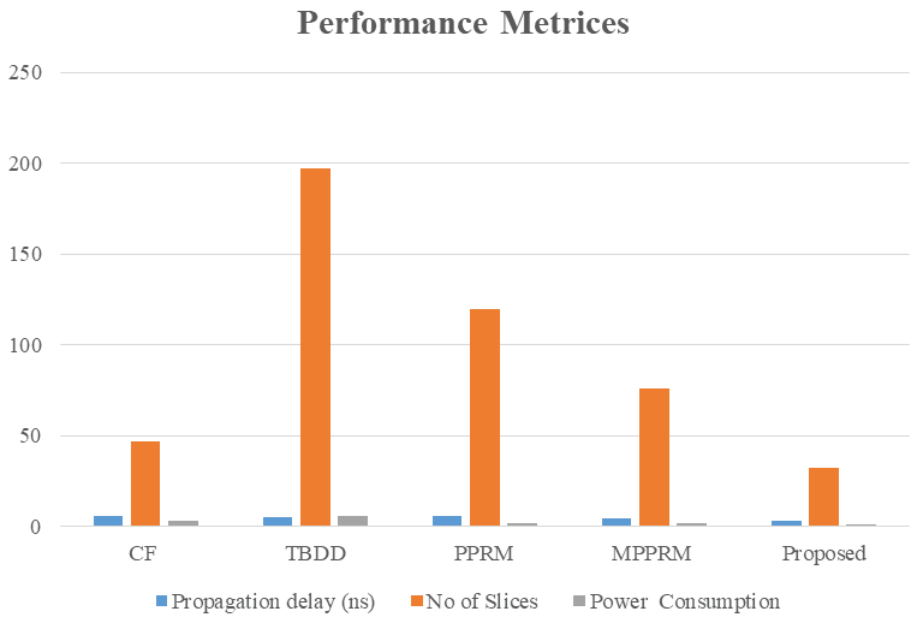

Figure 9. Comparative analysis of proposed model with traditional method.

The Figure 9, Figure10 and Table 2 signifies the comparative analysis of the presented mechanism with the classical approach. It is identified that the proposed system outperforms the existing model by attaining a maximum of 2.91 and a minimum of 1.456 lesser delay values, a maximum of 165 slices, and a minimum of 25 slices lesser amount

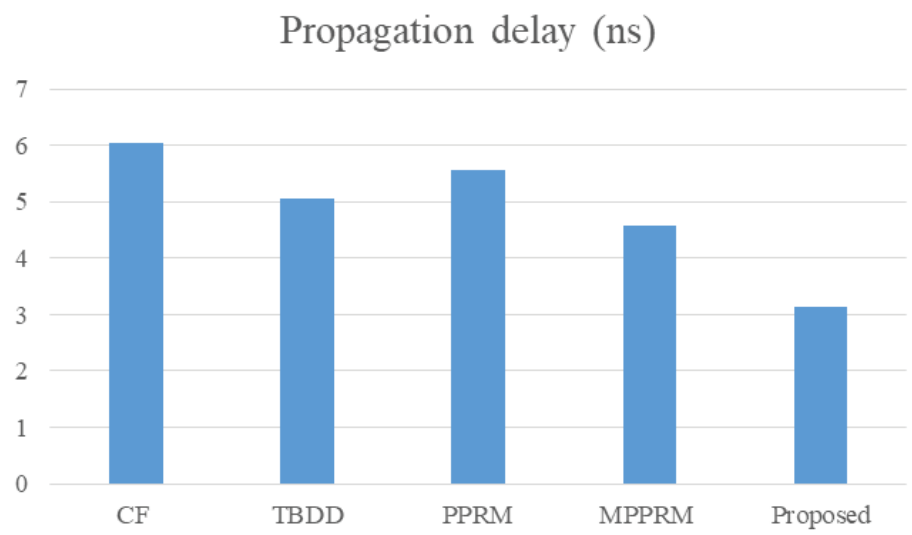

Figure 10. Comparative analysis of projected model with existing method.

Table 3. Comparative analysis of presented system with conventional model

Scheme	Critical path time (ns)	Throughput	power (mW)
NIST	5.68	175.8	47.94
DOR	4.62	216.3	23.33
Dual stageT	3.63	277.4	13.21
Proposed	**2.04**	**312**	**10.78**

of slices value. Besides, it accomplishes a maximum of 1.98 w and a minimum of 0.546 w, lesser power consumption than the conventional method, which represents the greater efficacy of the presented approach. Correspondingly, Table 3 and figure.11 depicts the comparative analysis of the proposed system with the existing model.

Figure 11 and Table 3 signify the comparative analysis of the projected system with the classical model. From the analysis, it is identified that the presented approach

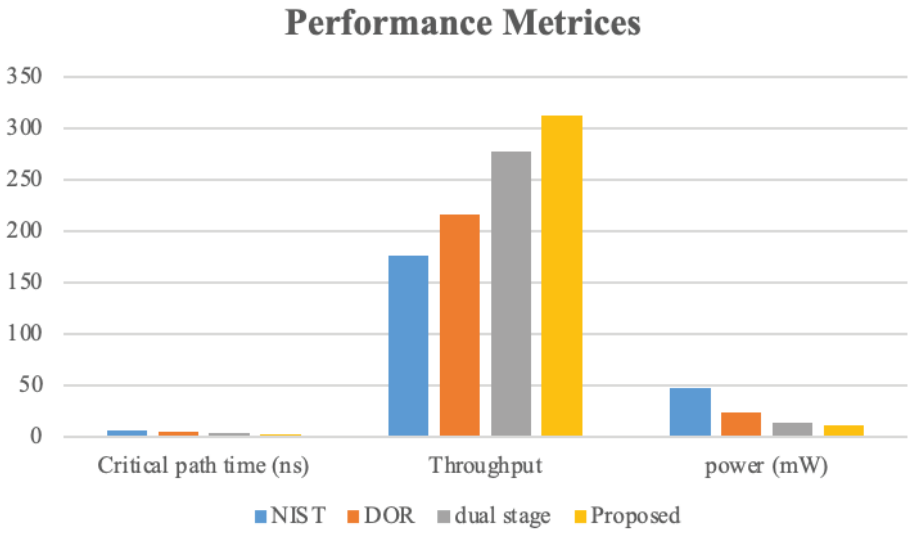

Figure 11. Comparative analysis of suggested model with existing method.

Table 4. Comparative analysis of proposed system with traditional model

Existing models	Devices	Slices	Max.Frequency (Mhz)	Throughput (Gbps)	Throughput/Area (Mbps/Slice)
[14]	Virtes-6 xc6vlx240t	32	699.37	5.57	170
This work	Virtes-6 xc6vlx240t	31	724.638	5.79	187
[12]	Virtes-5 xc5vlx20t	36	571.91	4.57	126
[16]	Virtes-5xc5vlx50t	31	512.821	4.102	132
[17](non pipeline)	Virtes-5 xc5vlx20t	34	303.79	2.43	71
[17](pipeline)	Virtes-5 xc5vlx20t	37	571.91	4.575	124
[18](non pipeline)	Virtes-5 xc5vlx20t	32	523.56	4.188	131
[18] (pipeline)	Virtes-5 xc5vlx20t	35	617.25	4.938	141
This work	Virtes-5 xc5vlx20t	17	644.33	5.514	303
[15]	Virtes-4 xc4vf100	45	209.61	1.68	37
This work	Virtes-4 xc4vf100	48	549.753	4.39	91
[13]	spartan-3 xc3s200	69	327.22	2.62	38
This work	spartan-3 xc3s200	63	338.295	2.71	43
Proposed	**spartan-3 xc3s200**	**62**	**328.295**	**2.86**	**26**

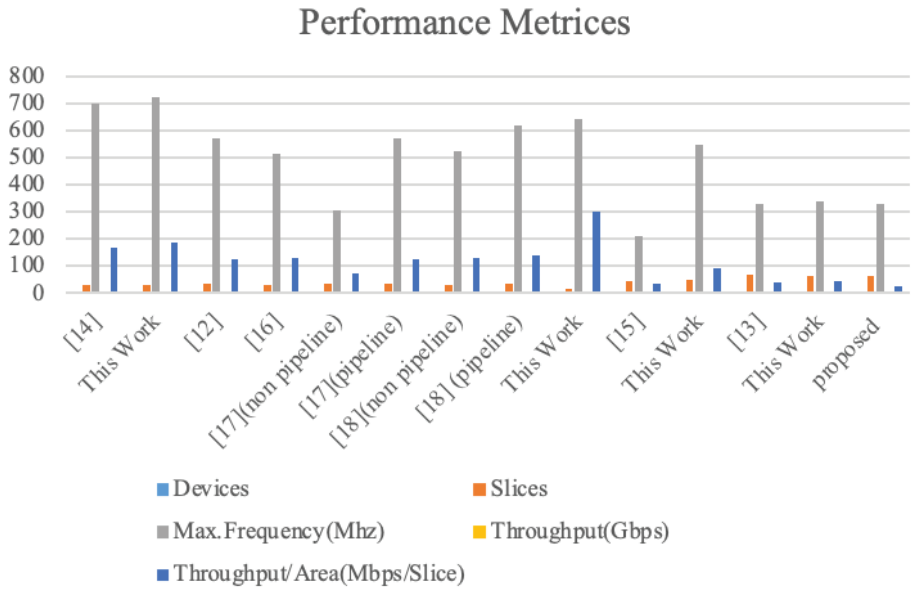

Figure 12. Comparative analysis of respective approach with classical method.

accomplishes a maximum of 3.64 and a minimum of 1.56, less than the classical approach. Similarly, it attained a maximum of 136.2 and a minimum of 34.6, greater throughputs than the traditional mechanisms. In the same way, for power consumption value, it attained a maximum of 37.16 and a minimum of 2.43, lesser than the pioneering approach, which represents the better performance of the respective research. Correspondingly, table.4 and Figure.12 signify the comparative analysis of the presented system with the conventional model.

Figure 12 and Table 4 depict the comparative analysis of the projected model with the traditional approach. The outcome of the comparative analysis represents the suggested method attained a minimum of 12 and a maximum of 277, lesser than the traditional methods. Therefore, the proposed method attained better efficiency than the conventional system. Similarly, Table 5 and Figure.13 signify the comparative analysis of the respective approach with the classical system.

Table 5. Comparative analysis of presented system with existing model

Method	Block size (bit)	Key size (bit)	Cycles per encryption	Area (k GEs)	Working freq. (MHz)	Power (µW)	Throughput (Mbps)	Normalized power (µW)
Existing	128	128	186	5.4	10	10.01	6.88	10.01
Proposed	**128**	**128**	**192**	**3.2**	**8.23**	**8.23**	**3.33**	**8.23**

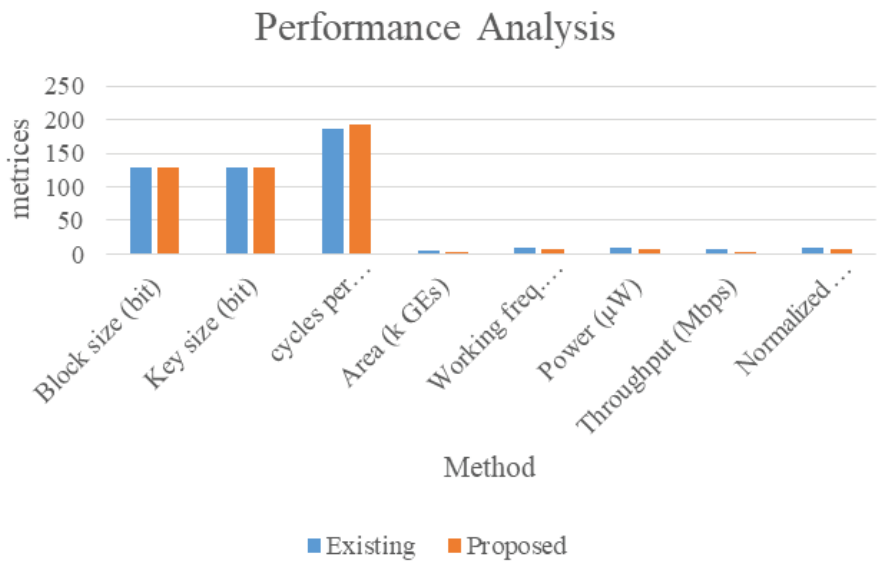

Figure 13. Comparative analysis of proposed system with traditional technique.

Table 5 and Figure 13 denote the comparative analysis of the projected system with existing research. From the analysis, it is identified that the suggested model attained 3.55 lesser throughput and 1.78 lesser power consumption than the conventional model. Therefore, the outcome of the comparative analysis represents the better efficiency of the proposed model.

Correspondingly, respective research utilized the advantages of ADCNN for the TCAM error correction and attained better performance with an efficiency value of 97%, delay of 3.066, area of 4.156, and power consumption of 31.605 w. Moreover, comparative analysis results reveal the greater performance of the presented system. Consequently, proposed research in the error correction in TCAM with ADCNN attained better performance, which is verified through the results.

CONCLUSION

The IC3-FPGA is a particular type of FPGA that can be configured and reconfigured with diverse digital logic functions for various applications like communication and networking, digital signal processing, medical devices, etc. The TCAM component in the FPGA is utilized for effective content-aided searching, high-speed pattern matching, or other functions. However, errors in TCAM can affect the outcome of the search process with inconsistent and incorrect pattern matching and can lead to routing errors and dropped packets. It is essential to correct the errors in TCAM to enhance the efficiency of system performance. To overcome the TCAM error, several conventional researchers attempted to attain better performance in the TCAM error correction. Nevertheless, lacks significant metric efficiency, power consumption, throughput, etc. To resolve the issue, the proposed system utilized ADCNN to enhance the efficiency of TCAM error correction. The CNN is utilized for the capability of localized weight sharing, translation invariances, etc. To resolve the limitation of long-term dependencies in the projected system, the ADCNN model is used in the proposed method. The input is the gate level inputs in the TCAM, where the outcome is the error-corrected TCAM. Correspondingly, the performance of the proposed TCAM error correction is calculated using metrics such as area, power, and delay. Accordingly, the result of the respective research signifies that the presented approach attained an efficiency of 97%, area of 4.156, power consumption of 31.605W, and delay of 3.066. Moreover, the outcome of the comparative analysis exposes the greater efficiency of the proposed method. Substantially, in the future, the respective system can be improved by enhancing the efficiency value.

ACKNOWLEDGEMENTS

We would like to express our gratitude to the reviewers for their precise and succinct recommendations that improved the presentation of the results obtained.

AUTHORSHIP CONTRIBUTIONS

Author equally contributed to this work.

DATA AVAILABILITY STATEMENT

The author confirm that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

REFERENCES

[1] Irfan M, Yantır HE, Ullah Z, Cheung RC. Comp-TCAM: An adaptable composite Ternary content-addressable Memory on FPGAs. IEEE Embedded Syst Lett 2021;14:63-66. [CrossRef]

[2] Zhang R, Tang C, Sun X, Li M, Jin W, Li P. Sky-TCAM: Low-power skyrmion-based ternary content addressable memory. IEEE Trans Electron Devices 2023;70:3517-3522. [CrossRef]

[3] Pan K, Tosson AM, Wang N, Zhou NY, Wei L. A novel cascadable TCAM using rram and current race scheme for high-speed energy-efficient applications. IEEE Trans Nanotechnol 2023;22:214-221. [CrossRef]

[4] Irfan M, Ullah Z, Cheung RC. D-TCAM: A high-performance distributed RAM based TCAM architecture on FPGAs. IEEE Access 2019;7:96060-96069. [CrossRef]

[5] Irfan M, Ullah Z, Chowdhury MH, Cheung RC. RPE-TCAM: Reconfigurable power-efficient ternary content-addressable memory on FPGAs. IEEE Trans Very Large Scale Integr (VLSI) Syst 2020;28:1925-1929. [CrossRef]

[6] Sadeh Y, Rottenstreich O, Kaplan H. Optimal weighted load balancing in TCAMs. IEEE/ACM Trans Netw 2022;30:985-998. [CrossRef]

[7] Narla S, Kumar P, et al. Modeling and design for magnetoelectric ternary content addressable memory (TCAM). IEEE J Explor Solid-State Computat Devices Circuits 2022;8:44-52. [CrossRef]

[8] Ullah I, Yang J-S, Chung J. ER-TCAM: A soft-error-resilient SRAM-based ternary content-addressable memory for FPGAs. IEEE Trans Very Large Scale Integr (VLSI) Syst 2020;28:1084-1088. [CrossRef]

[9] Suresh MK, Bhanu K. Error detection and correction in SRAM emulated TCAMs. J Eng Sci 2023;14.

[10] Garzón E, Golman R, Lanuzza M, Teman A, Yavits L. A low-complexity sensing scheme for approximate matching content-addressable memory. IEEE Trans Circuits Syst II Express Briefs 2023;70:3867-3871. [CrossRef]

[11] Muskan SM, Govindarajulu S. Implementation of parallel TCAM with soft-error-resilient SRAM for high-scalability search applications. J Eng Sci 2022;13.

[12] Sakthi K, Nirmal Kumar P. Minimizing subtle errors in computing information of TCAM by partial "N" search key implementation. Int J Uncertain Fuzziness Knowl-Based Syst 2022;30:169-184. [CrossRef]

[13] Bukkapatnam K, Singh J. Design of parallel memory allocation using error resilient ternary content-addressable memory for fast error correction. Turk Online J Qual Inq 2021;12.

[14] Prasanthi E, Neha S, Manasa T, Anunya S, Sudeepthi V, Chandrakala S. Design of LFSR based fast error-resilient ternary content addressable memory. Turk J Comput Math Educ 2023;14:472-481.

[15] Pourmeidani H, Habibi M. A range matching CAM for hierarchical defect tolerance technique in NRAM structures. arXiv Prepr arXiv:1907.04504 2019.

[16] Merlin I, Garzón E, Fish A, Yavits L. DIPER: Detection and identification of pathogens using edit distance-tolerant resistive CAM. IEEE Trans Comput 2023;73:2463-2473. [CrossRef]

[17] Yadav CS, Sandhya R. A ternary based soft error resilient SRAM content addressable memory with improved security using checksum method. Int J Modern Trends Sci Technol 2022;8:116-121.

[18] Duggeboina E, Surekha PS, Srinivas K. Error resilience in LFSR-based ternary content-addressable memory on FPGAs for packet classification in SDN and OpenFlow. Turk J Comput Math Educ 2020;11:2415-2424.

[19] Vineetha K, Sasikala E. Design of fault tolerant and high speed TCAMs in FPGA.

[20] Bhulakshmi K, Krishna MH. An efficient error correction system in SRAM ternary content-addressable memories by using software defined networks. 5th International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech).

[21] Garzón E, Yavits L, Finocchio G, Carpentieri M, Teman A, Lanuzza M. A low-energy DMTJ-based ternary content-addressable memory with reliable sub-nanosecond search operation. IEEE Access 2023;11:16812-16819. [CrossRef]

[22] Syafalni I, Adiono T. Optimized multiple-bit-flip soft-errors-tolerant TCAM using machine learning. Jurnal Nas Tek Elektro 2022:36-42. [CrossRef]

[23] Yavits L. Hamming distance tolerant content-addressable memory (HD-CAM) for approximate matching applications. arXiv:2111.09747v1 [cs.AR] 18 Nov 2021.

[24] Wang C, Zhang D, Zeng L, Zhao W. Design of magnetic non-volatile TCAM with priority-decision in memory technology for high speed, low power, and high reliability. IEEE Trans Circuits Syst I Regul Pap 2019;67:464-474. [CrossRef]

[25] Bukkapatnam K, Singh J. VLSI implementation of low-power and area efficient parallel memory allocation with EC-TCAM. Integration 2022;87:336-345. [CrossRef]