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Research Article

Narrowband and highly linear LNA design for 4.5 GHZ on 180NM CMOS

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ABSTRACT

In this paper, a narrowband and highly linear Low Noise Amplifier (LNA) is designed and implemented on 180 nm CMOS technology, operating at a center frequency of 4.5 GHz. This LNA design is particularly suitable for modern communication systems and emerging 5G applications. For simulation and analysis, the 180 nm Generic Process Design Kit (GPDK) in Keysight's Advanced Design System (ADS) was utilized. To improve stability and gain, resistive feedback was chosen, while inductive source degeneration was employed to achieve better noise performance and linearity. The proposed design aims for a simple architecture, and its narrowband specifications are achieved through optimized input and output matching networks. The analysis showed that the designed LNA provides a gain of 14.1 dB, a minimum noise figure of 0.928 dB, an input 1-dB compression point (P1dB) of 0 dBm, and an input third-order intercept point (IIP3) of 4.942 dBm across a 360 MHz band. These results indicate excellent linearity and signal integrity, and show the design is competitive with relative studies. The novelty of this work lies in achieving high linearity and low noise with a notably simplified design, overcoming common trade-offs. Compared to recent state-of-the-art work, the proposed LNA offers superior linearity and a lower noise figure while maintaining a simple circuit topology.

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INTRODUCTION

Wireless communication systems have become an essential part of our lives for a very long time. Over time, the needs and specifications expected from these systems became more and more advanced. This trend led the subsystems and components to evolve to provide the performance requirements. The receivers used in these systems employ many components. Low noise amplifiers (LNA) are one of the most important parts of wireless receivers [1]. Their main role is to amplify the received signal while adding minimal noise to it. This enables them to improve the quality of the signal in terms of the signal-to-noise ratio (SNR) [2]. It also offers non-linearity to the circuit since it is an active device. The LNA's non-linearity is undesired since it leads to signal

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distortion and the generation of undesired products like harmonic and inter-modulation distortion [3]. In order to overcome the non-linearity, a filter prior to the LNA is placed to suppress the unwanted bands. These filters are also crucial for noise figure calculations since cascaded noise figure calculations show that the first element of the network provides the most significant contribution to noise [4]. Therefore, it is important to have a low noise figure (NF) in the first element of the receiver, which is typically a passive band-select filter that introduces a noise equal to its insertion loss [5]. This condition leads to a trade-off between selectivity and the total NF of the receiver. To overcome the high NF contribution issue of band select filters, various different types of band selective or narrowband LNA designs were offered [6-9]. These studies offer varied solutions like frequency translational resistive feedback architectures, current conveyors, nested reactive feedback loops, and integrated frequency selective networks. These designs were mainly focused on complex topologies such as multistage matching circuits, baluns, and feedback networks to provide better selective characteristics. Since the filter is not used in these designs to lower the unwanted frequency components, the linearity of the designed LNA becomes more decisive in terms of performance. Yet, the linearity of the designs mostly was not prioritized as a design goal. On the other hand, regular LNA studies focusing on these bands are focused on either the noise figure or the linearity improvements by making trade-offs on the non-focused side. This approach led to bad affection for their overall performance.

In this paper, a narrowband and highly linear LNA design was implemented to overcome the trade-off between noise figure and selectivity. The design is made for a rather less popular band which is reserved for military communications and future 5G communication systems, 4.5 GHz [10,11]. To minimize complexity, size, and cost, maintaining circuit simplicity was a key design objective. To provide better stability and matching characteristics, resistive feedback and source inductive degeneration techniques are employed within the design [12,13]. Input and output matching circuits, on the other hand, are designed to obtain a narrowband response by applying a simple network design with two elements. This design method provides simpler circuits in terms of components as well as offers a good band selectivity performance. The nonlinear behavior of the device is also taken into account within the design by determining the parameters of the components used. GPDK 180 nm process is used to implement the design in the Advanced Design System (ADS) of Pathwave Design to run S-parameter and nonlinear simulations.

THEORY

Design Objectives

Design objectives of the LNA design can be seen in Table 1.

Table 1. Design objectives of the Lna design

Specification	Unit	Value
Center frequency	MHz	4500
Bandwidth	MHz	350
Maximum noise figure	dB	<1.3
IP1dB	dBm	>-5
IIP3	dBm	>4
Minimum gain	dB	>11

The main objective is to have a frequency-selective response both on input and output matching circuits so the amplifier can also act close to a filter over the band. It is also aimed to have NF lower than 1.3 dB over the passband of the design while having a gain of more than 11 dB. Since the LNA is designed to act as a filter and therefore as the first element of a receiver structure, linearity objectives are also considered to be important. In order to obtain a linear characteristic, IIP3 values bigger than 7 dB and IP1dB values bigger than -5 dB are aimed to be achieved.

Transistor Sizing

RF field effect transistors (FET's) have lots of parameters which has a direct effect on the performance. In this study, the physical parameters of transistors which are length, width, and number of fingers, are selected to have the transistor optimized for the design objectives. The length of the transistor has an inversed relationship with the cutoff frequency (f_T) [14]. Formula for the f_T can be seen (1).

$$f_T = \frac{V_a}{2*\pi*C_{total}} \quad (1)$$

f_T represents the transition frequency or cutoff frequency, V_a is the Early voltage and C_{total} refers to the total capacitance of the transistor.

Unlike the f_T, the length of transistor has a direct relationship with the transconductance (g_m) of the transistor. In this design, the length of the transistor is picked as the minimum length the process can offer, 180nm. This selection was made to ensure the maximum high-frequency performance of the transistor.

The channel width of the transistor, on the other hand, is mainly effective on the current flow capability and physical coverage of the component on the layout [15]. This parameter was mainly considered to have sufficient power to obtain the nonlinear specifications of the amplifier.

The number of fingers to be used on the transistor is also an important parameter since it can provide additional improvement in terms of linearity and g_m [16,17] Yet, it should be noted that it can lead to performance degradation in terms of f_T. Depending on optimization results, 200 µm is chosen to be the length with 4 fingers in total to have a 50 µm finger width.

Topology

There are various topologies to form an LNA using a single transistor element. The most common of these topologies are common source and common gate amplifiers [18]. The main advantage of the common source is the minimized NF whilst the common gate topology offers more bandwidth due to the limited miller effect [19]. Since the objective is to have a narrowband response and low NF as possible, common source topology is used as the reference. The common source design topology can be seen in Figure 1. In this topology, the input signal is applied to the gate (G) and the amplified and inverted output signal is taken from the drain (D), with the source (S) terminal being common to both the input and output.

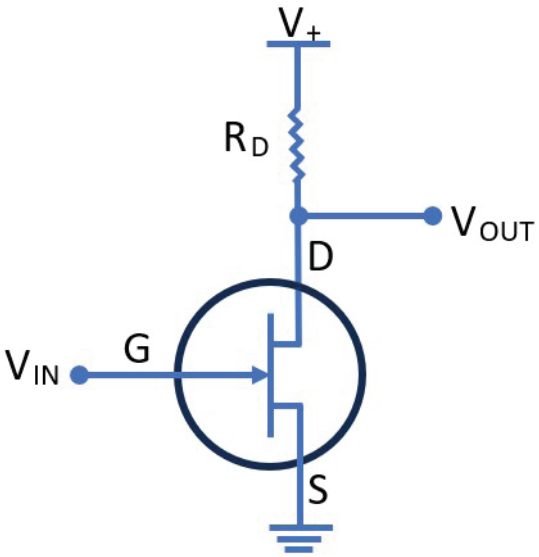


Figure 1. Common source topology.

After deciding the main topology, various techniques to be added to improve performance on different aspects such as stability, gain and bandwidth are also chosen. In order to obtain the unconditional stability of the transistor over the operating bandwidth, resistive feedback is added to the main topology. This addition also had its impacts on other parameters such as matching. Also to improve stability and noise characteristics over the operating band, the source inductive degeneration technique is chosen to be added in the topology. Matching circuits to be designed are mainly focused on obtaining selectivity in terms of the operating band while using a minimum number of components to avoid complexity and therefore large area occupation within the die. With the same concern regarding circuit size, lumped comments offered within the process which are MIM capacitors [20] and spiral inductors [21], will be used as elements of the matching network.

DESIGN

The design procedure of the LNA consists of analysis and considerations covering DC biasing, stability, S parameter analysis and matching network design.

DC Analysis

The chosen 50x4 μm width transistor's I/V curve analysis can be seen in Figure 2. The optimum biasing point is chosen to be at 0.7 V VGS and 2 V VDS, which stands as a valid point regarding the class A amplifier operating conditions [22].

The transconductance(gm) analysis at the selected bias point can be seen in Figure 3. The transconductance value is chosen to be 0.002 S for the design.

In order to calculate the DC power consumption of the proposed LNA, voltage and current values determined from the DC analysis can be used. The main reason behind

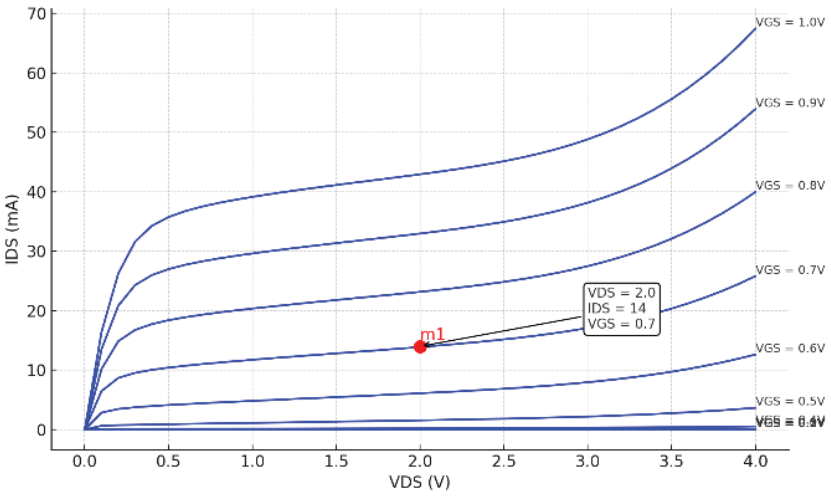


Figure 2. 50X4 μm transistor I/V curve analysis.

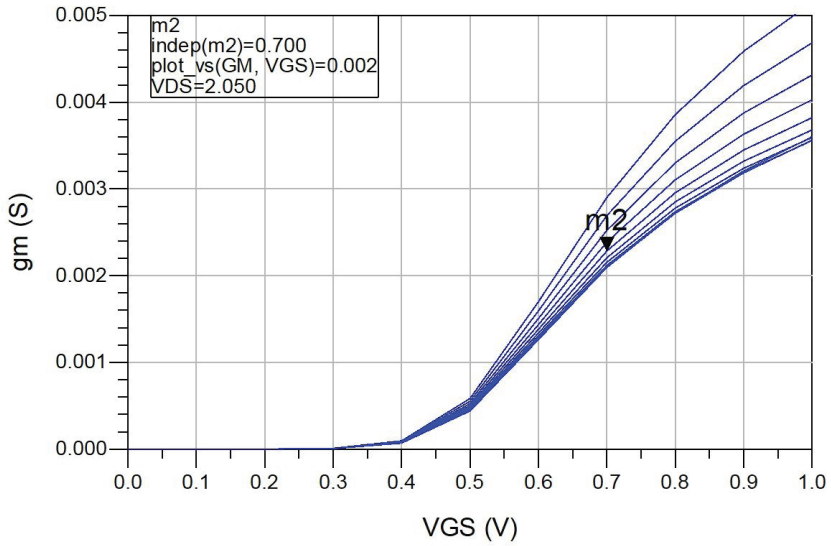


Figure 3. Transconductance analysis of the 50X4 μm transistor.

it is that the LNA is assumed to work with small signals which does not affect the bias point and operating region of the transistor.

DC power consumption can be calculated with formula (2).

$$P_{del} = I_D * V_{DS} \tag{2}$$

P_{del} represents the total DC power consumption, I_D is the drain current, and V_{DS} is the voltage applied to the drain. By using formula (2), DC power consumption can be calculated as 28 mW.

RF Analysis

After DC analysis, a biasing network is formed to get the design ready to stability and s parameter analysis. The design schematic can be seen in Figure 4. Due to the determinations made on design methodology, a source degeneration inductor and a feedback resistor are also added.

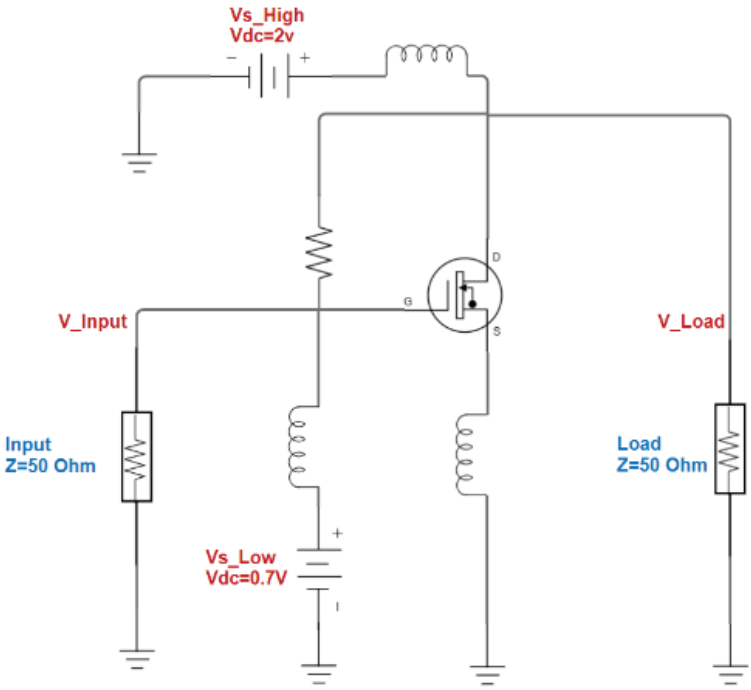


Figure 4. Design circuit schematic.

The circuit's stability analysis made for a wideband frequency range (2-6 GHz) can be seen in Figure 5. It is clear that the circuit is unconditionally stable within the operating bands (4-5 GHz).

S parameter analysis can be seen in Figure 6. Reverse isolation (S12) is low enough for unilateral consideration [23], and forward transmission parameters are within the needs of design objectives in 4.5 GHz.

Maximum gain analysis can be seen in Figure 7. It is clearly seen that this biasing condition provides enough gain for design objectives.

Matching

For matching network design, a narrowband frequency response is targeted by using a minimum number of components. Impedance points for optimum source, load and noise figure matching can be seen in a normalized smith chart for frequencies between 2-6 GHz in Figure 8.

For a target center frequency of 4.5 GHz with a narrow bandwidth (less than 10%), the matching networks must be highly frequency selective. On the Smith chart, this means that while the impedance should be perfectly matched at 4.5 GHz, it should move away from the center point at adjacent frequencies. Also, the source matching network must

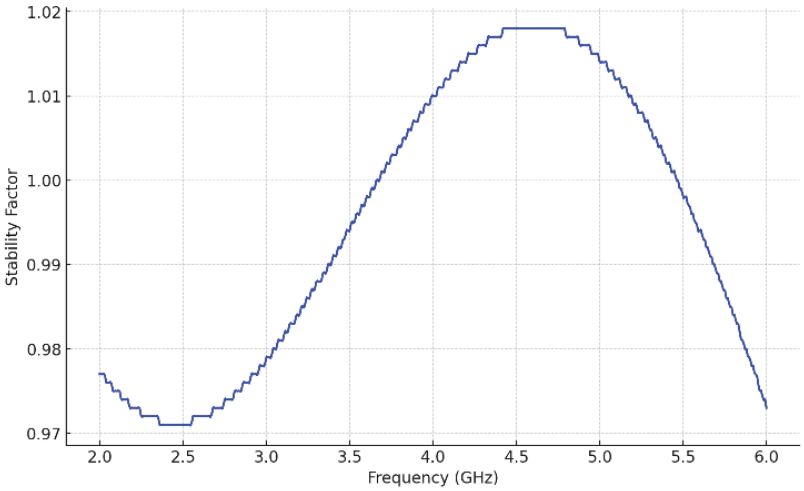


Figure 5. Stability analysis of the circuit.

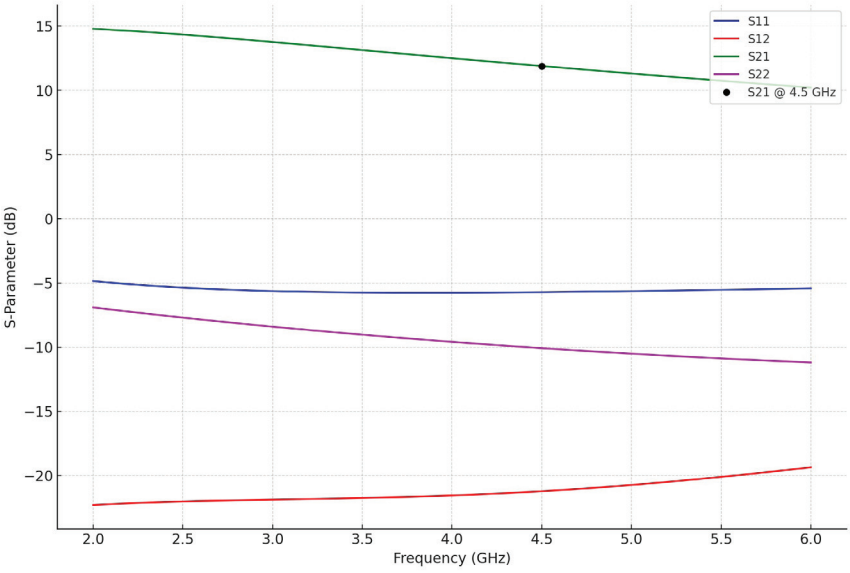


Figure 6. S parameter analysis of the circuit.

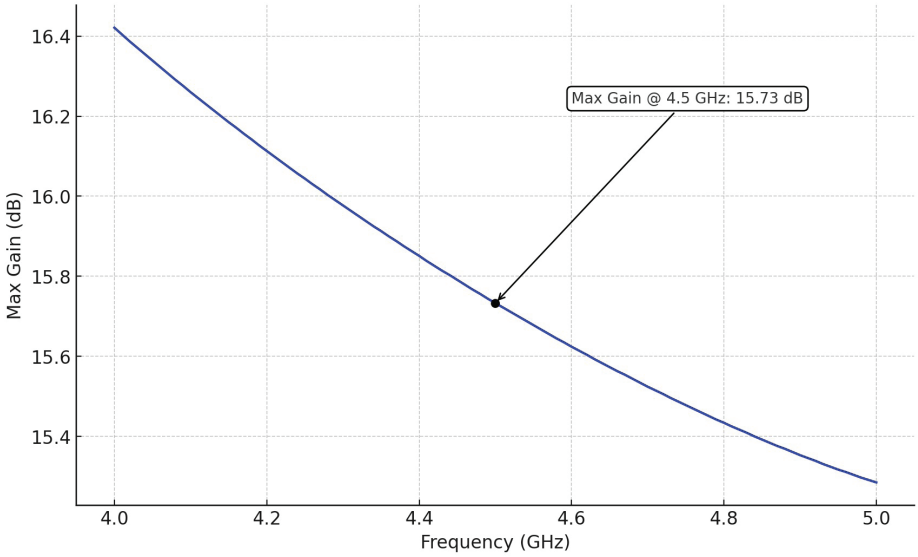


Figure 7. Maximum gain analysis of the circuit.

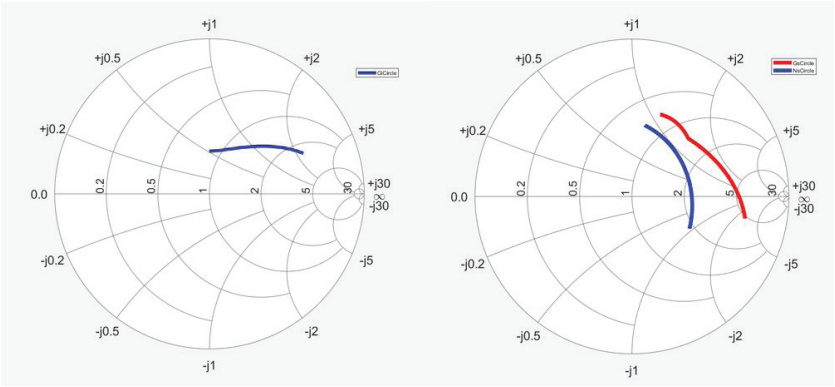


Figure 8. Impedance matching points of the circuit.

be designed to achieve an optimal trade-off between gain and noise figure, with a clear priority given to minimizing the noise figure.

To have all this, a simple series LC network was offered for both source and load matching. Series capacitance was needed to adjust the impedance points to R=1 circle and also to act as a DC block, and since the aimed matching points to obtain the objectives for 4.5 GHz is placed close enough to the R=1 circle, there are no additional parallel components used. A series inductor is good enough to match the reactance for both sides of the transistor. The chosen matching network can be seen in Figure 9. A spiral inductor and a MIM capacitor are chosen from the GPDK library to be used within the network. The parasitic of these devices were not dominant on the operating band and therefore, ignored within this design.

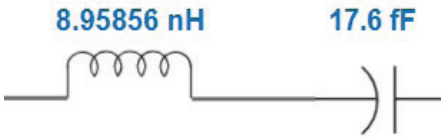


Figure 9. Matching network proposed for the LNA.

Reactance value of the selected capacitor value (17.6 fF) can be calculated with formula (3).

$$X_C = \frac{1}{2*\pi*f*C} \tag{3}$$

X_C represents the reactance value of capacitor, f is the frequency, and C is the capacitance value. For the capacitor on the source and load matching circuits (17.5 fF), reactance value can be calculated as 2012 Ω. High reactance value allows the impedance values to be adjusted on R=1 circle.

Reactance value of the selected inductor values (8.269 nH and 8.958 nH) can be calculated with formula (4).

$$X_L = 2 * \pi * f * L \tag{4}$$

X_L represents the reactance value of inductor, f is the frequency, and L is the inductance value. For the inductor on the source matching circuits (8.958 nH), reactance value can be calculated as 253.1 Ω. On the load matching circuit, the inductor's (8.269 nH) reactance value is equal to 233.77 Ω. Both inductors have reactance values close to each other, which indicates that the impedances of source and load branches are close to each other.

Final Circuit

In the final design stage, all passive and active components were integrated to form the complete LNA circuit. The finalized schematic, shown in Figure 10, incorporates the biasing network, stabilization elements, and matching circuits. The spiral inductors and MIM capacitors used are selected from the GPDK library due to their compact footprint and acceptable Q factor in the 4–5 GHz range. The values for all components used in the LNA are summarized below. These values are derived based on impedance transformation requirements, stability goals, and noise figure optimization. Calculations were carried out using standard L-network synthesis equations and Smith chart mappings. The source and load matching networks are tuned specifically to target the 4.5 GHz center frequency with a fractional bandwidth of less than 10%. After the implementation of matching networks, the final circuit design was complete and can be seen in Figure 10. The values of the components used are summarized in Table 2.

Table 2. Component values used in Lna design

Name/Indicator	Unit	Value
Feedback resistor	Ω	1050
Source inductor	pH	215.49
Drain inductor (RF choke)	nH	42.13
Gate inductor (RF choke)	nH	8.367
Source matching inductor	nH	8.958
Source matching capacitor	fF	17.6
Load matching inductor	nH	8.269
Load matching capacitor	fF	17.6

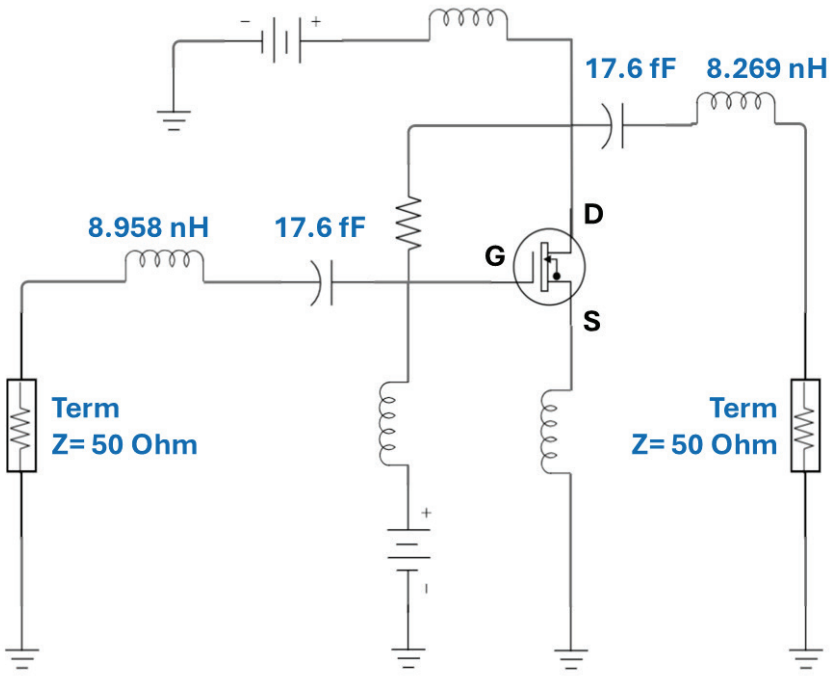
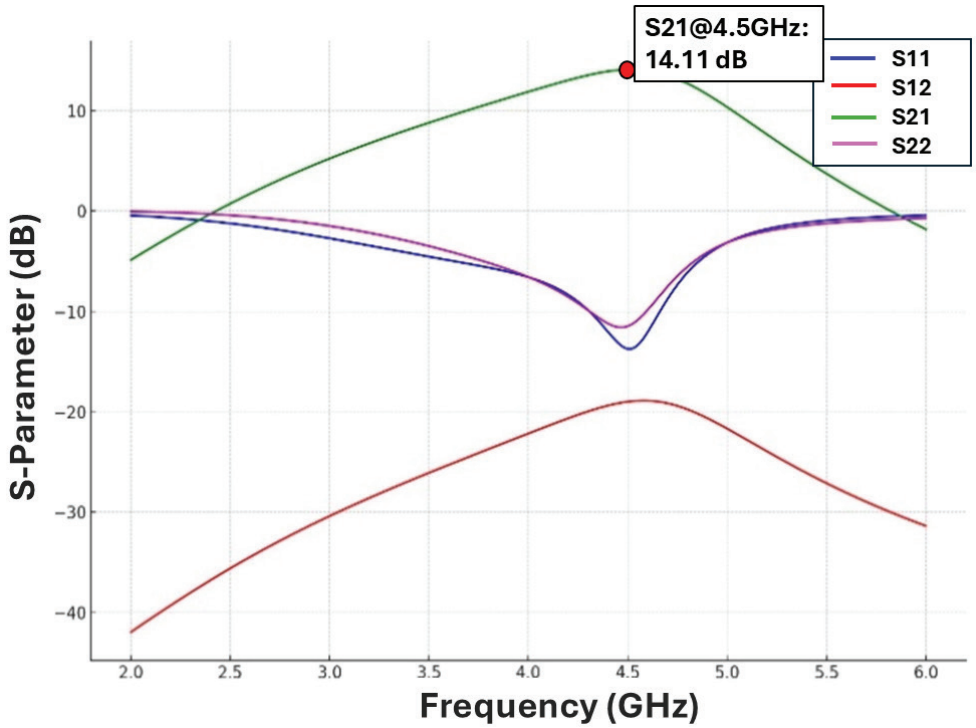


Figure 10. Final circuit of the LNA design.

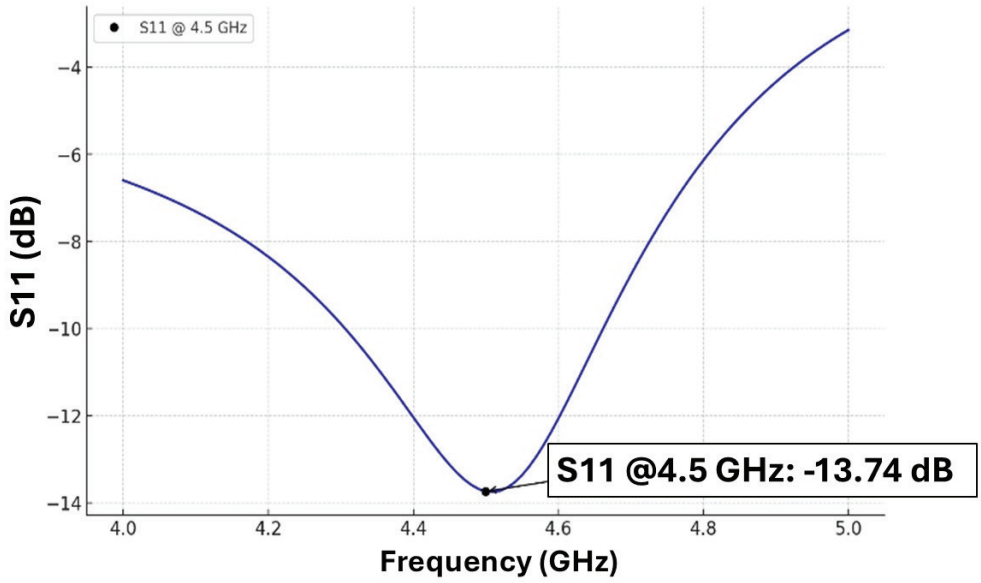
RESULTS AND DISCUSSION

Linear and Noise Performance

Simulations are created both for the linear and nonlinear characteristics of the LNA. In order to check the linear characteristics, S parameter analysis results can be observed in Figure 11(a). The gain is measured as 14.105 dB. To measure the performance of the LNA input matching, the S11 value was checked if it is below -10 dB. Detailed analysis of S11 can be seen in Figure 11(b). From the measurement, it can be said that the LNA input matching bandwidth is around 360 MHz. Noise figure simulation results can be seen in Figure 11(c). The noise figure acquired for 4.5 GHz is almost equal to the minimum noise figure, 0.928 dB, which is lower than the design objective.



(a)



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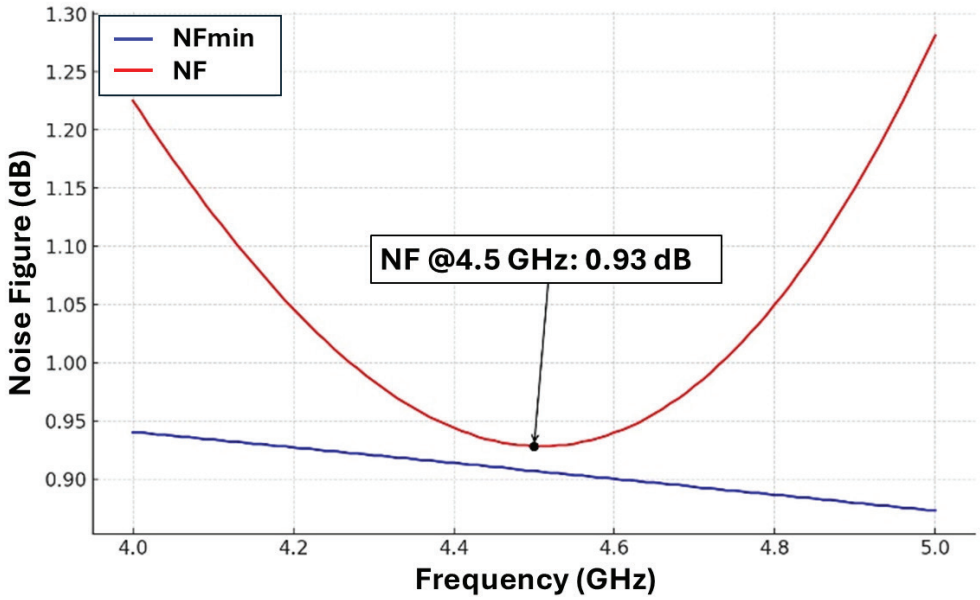


(c)

Figure 11. Linear and noise performance of the LNA: (a) S parameters of the LNA (b) S11 analysis of the LNA. (c)Noise figure analysis of the LNA.

Matching Network Analysis

In order to observe the effectivity of the designed matching networks, the impedance points shown in Figure 8. are analyzed and can be seen in Figure 12. It is shown that a successful discrimination between the optimal impedances of frequencies is achieved.

Nonlinearity Analysis

In terms of nonlinearity, P1dB and IIP3 parameters are analyzed. The gain over input power graph is shown in Figure 13. From the compression point, P1dB is found close to 0 dBm.

Multi-tone simulations are also analyzed to measure the IIP3 of the LNA. The results can be seen in Figure 14. OIP3 of the LNA is measured as 19.047 dBm for lower tone. Regarding the gain (14.105 dB) IIP3 can be calculated as 4.942 dBm. Results gathered from simulations are compared to similar studies in Table 3.

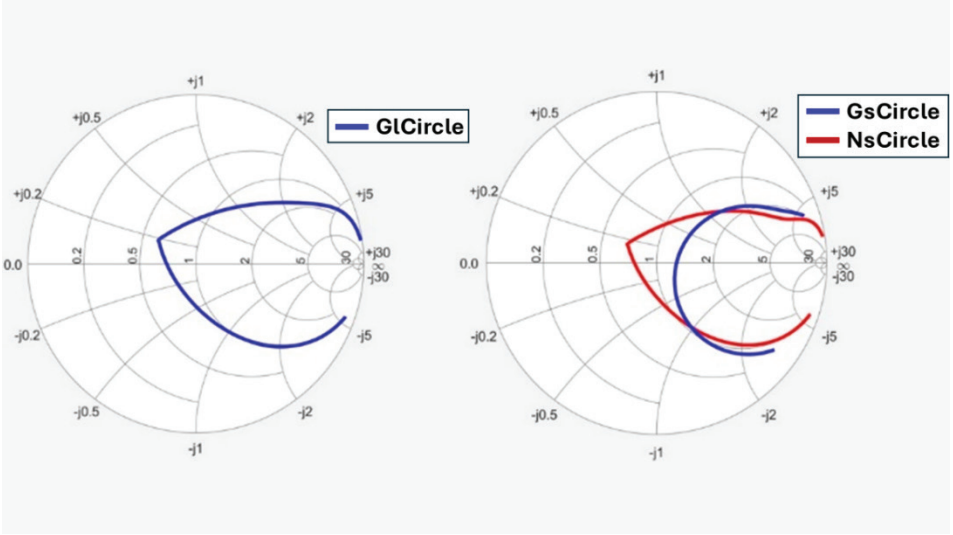


Figure 12. Smith Chart Analysis of the LNA.

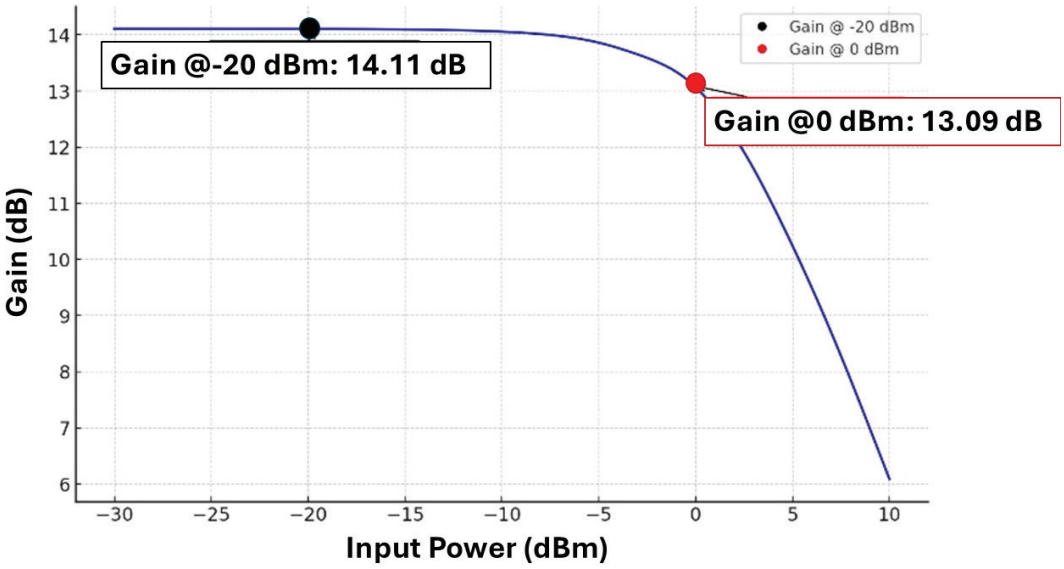


Figure 13. P1dB Analysis of the LNA.

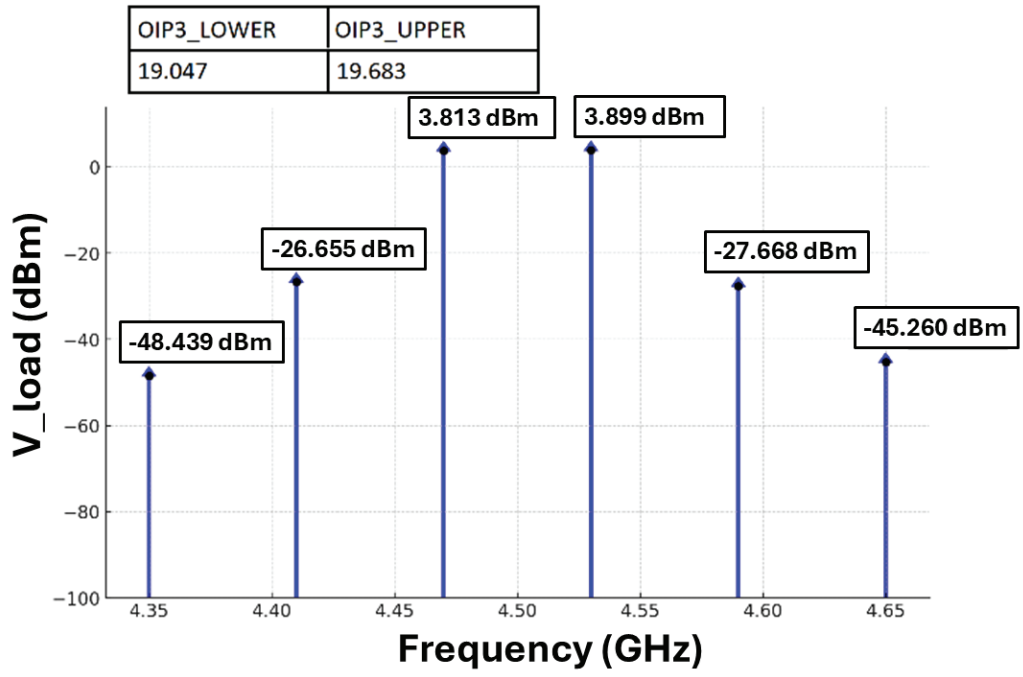


Figure 14. Multi tone analysis of the LNA.

The gain, noise figure, IIP3, and P1dB values from the LNA studies are visually compared in Figure 15(a), 15(b), 15(c), and 15(d), respectively.

Comparison with Other Studies

Results from this work and earlier studies [24-35] can be compared in various types of specifications.

By comparing the parameters provided, it can be said that the proposed design offers significantly higher linearity compared to most of the prior studies. Only two studies offer better linearity than the proposed design [33, 34].The study that stands to be better among all [33], has an IIP3 of 21 dBm and an IP1dB of 9 dBm. However, it exhibits a relatively high noise figure of 1.3 dB compared to this work, which offers 0.928 dB of noise figure. A similar situation applies to [34], which also demonstrates relatively good linearity. Although this work offers much higher gain

Table 3. Comparison of the Lna with other studies

Ref	Year	GPDK	Topology	Freq. (GHz)	Bandwidth (MHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	IP1dB (dBm)
[24]	2021	180 nm	Cascaded CSA	2.4	~400 MHz	19	0.5	-15.87	-26
[25]	2019	180 nm	Cascaded CSA	5	Not Given	24.65	0.794	-26.81	-36.11
[26]	2022	180 nm	Cascode CSA	2.4	~600 MHz	22.75	1.75	-13	-19
[27]	2023	180 nm	CSA	5.5	~200 MHz	12.S1	2.8	-18.7	-14
[28]	2022	180 nm	CSA	1-7	~6000 MHz	17.95	1.11	Not Given	Not Given
[29]	2023	90 nm	CSA	4.4–5.0	~600 MHz	20.6–19.9	1.57–1.73	−15.4	Not Given
[30]	2019	180 nm	Cascode CSA	6	~200 MHz	15.9	0.92	-1.1	-8
[31]	2022	180 nm	Cascode CSA	2.4	~820.3 MHz	21.5	0.506	0.513	-8.17
[32]	2021	180 nm	Differential CSA	1.9-4.5	~2300 MHz	12.3	2.6	-2.5	Not Given
[33]	2019	250 nm	CSA	5-6	~2000 MHz	14	1.3	21	9
[34]	2021	22 nm	Cascode CSA	2.4-5.25	~2850 MHz	30	1.49	9	3
[35]	2024	150 nm	Cascaded CSA	2.8–3.8	~1000 MHz	35.5	1-1.8	Not Given	-25.5
This work	**2024**	**180 nm**	**CSA**	**4.5**	**~360 MHz**	**14.1**	**0.928**	**4.942**	**0**

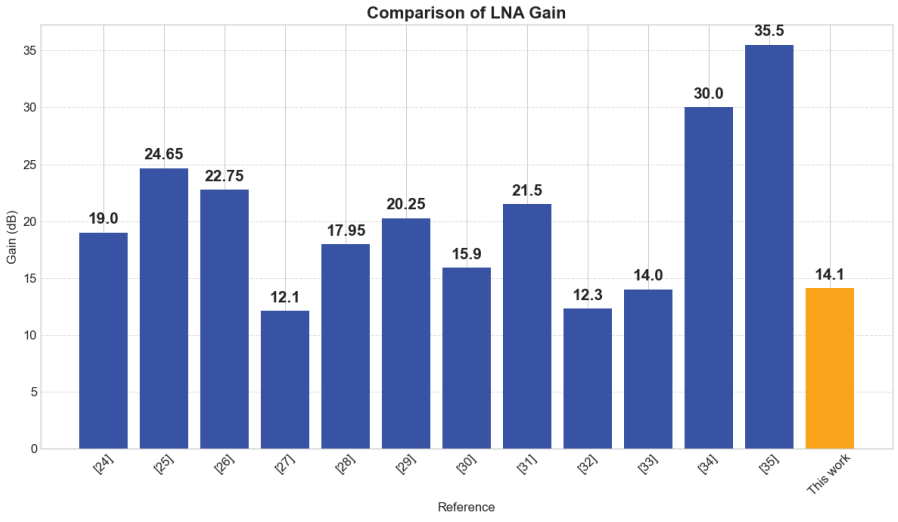
compared to the proposed design, it suffers from a wideband response, whereas the proposed design is more suited for narrowband applications.

In terms of noise figure (NF), there are some studies that offer better performance [24, 25, 30, 31] then this work does. Yet all of them fall short in terms of linearity. The best among these shows an IIP3 of -8 dBm and an IP1dB of -1.1 dBm, which are considerably worse than the proposed design.

In terms of gain, which is not the primary specification for this work to dominate over, there are various studies that offers better performance than the proposed design. Yet, none of these studies can offer the linearity and NF performance of the proposed design offers. From that perspective, it is fair to say that the proposed design successfully balances all critical performance parameters linearity, noise figure, and gain while offering simplicity through its topology.

Simulation Limitations

It must be noted that due to the nature of GPDK (Generic Process Design Kit), post-layout simulation results cannot be presented. This is due to GPDK not offering all layout components that are essential for layout design. This also caused the inability to make PEX (layout parasitic extraction) for this design. It is also not possible to make an accurate silicon area estimation due to this limitation. Yet, as mentioned earlier in the paper, parasitic values of



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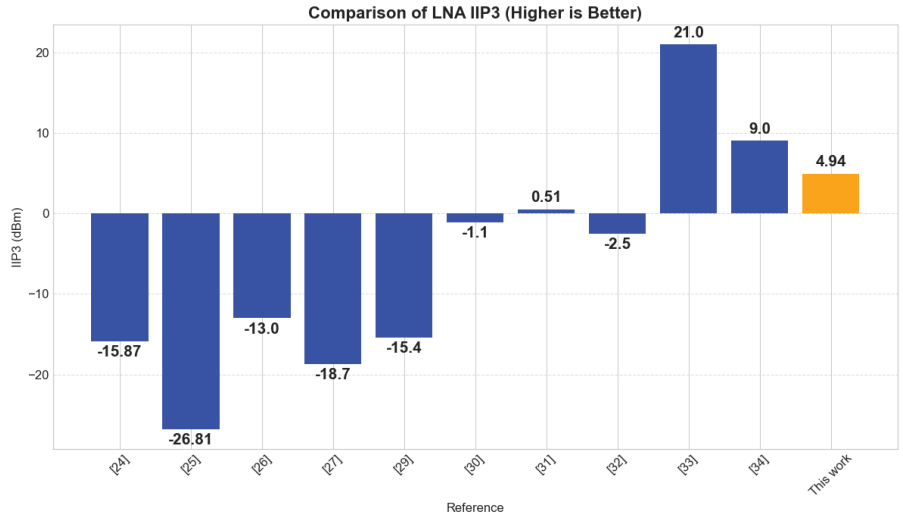

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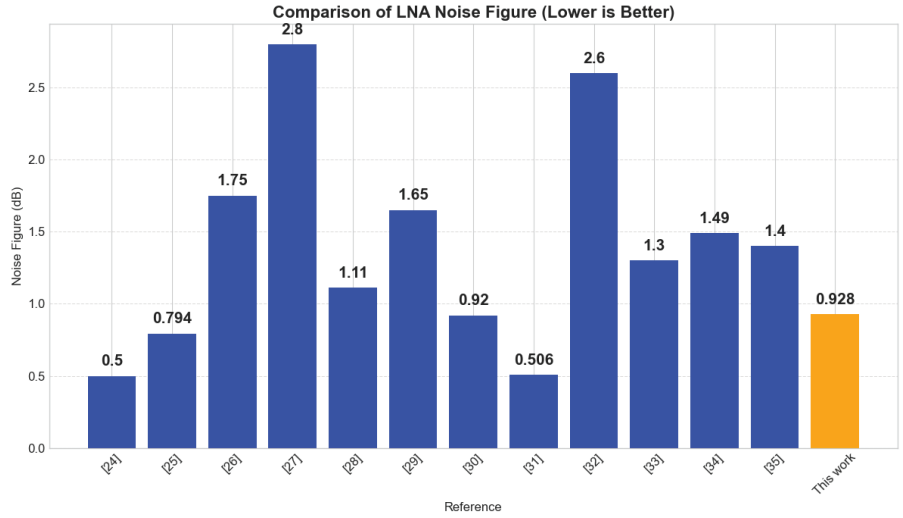

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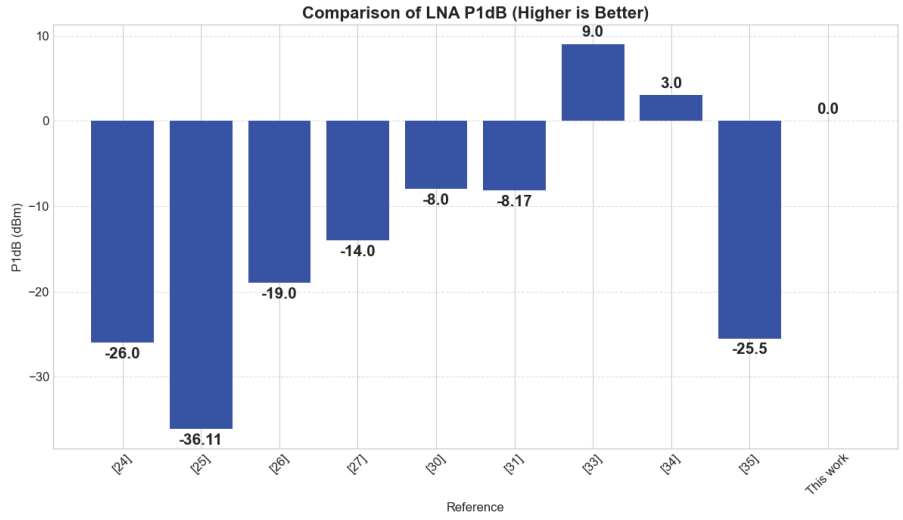

(d)

Figure 15. Performance comparison of this work with other LNA studies: (a) Comparison of Gain Values. (b) Comparison of IIP3 Values. (c) Comparison of Noise Figure Values. (d) Comparison of P1dB Values.

inductors, resistors and capacitors are checked in the early phases in the design and observed to be ineffective in terms of performance of the circuit.

CONCLUSION

In this paper, a narrowband and highly linear low-noise amplifier was designed within the common source topology by using the GPDK 180 nm process in ADS. Resistive feedback and source inductive degeneration methods were employed to improve stability and linearity. The topology was designed in such a way as to simplify the circuit by minimizing the number of components. Simulations indicated that the proposed design successfully covered 360MHz of bandwidth in 4.5 GHz while offering 0.912 dB noise figure, 14.1 dB gain, 0 dBm IP1dB and 4.942 dBm IIP3. These values show that the design offers better overall performance than the relative studies.

It must be emphasized that these results are based solely on pre-layout simulations. The limitations of the Generic Process Design Kit (GPDK) prevented post-layout extraction and analysis, meaning that parasitic effects from physical layout, process variations, and packaging are not accounted for in these results.

Despite this limitation, the results of this study successfully highlight the possibility of designing an LNA that combines both high linearity and simplicity. This combination is valuable for designers, as achieving good performance with fewer components contributes to creating cost-effective and robust systems.

NOMENCLATURE

f_T	*Cut-off Frequency*
V_a	*Early Voltage of The Transistor*
C_{total}	*Total Capacitance of The Transistor*
g_m	*Transconductance*
Ω	*Ohm*

AUTHORSHIP CONTRIBUTIONS

Authors equally contributed to this work.

DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

STATEMENT ON THE USE OF ARTIFICIAL INTELLIGENCE

Artificial intelligence was not used in the preparation of the article.

REFERENCES

[1] Duman M. Low noise amplifier design for hidden wireless LAN applications using band pass filter with geometric mean prototype element values. Sigma J Eng Nat Sci 2024;42:383–389. [CrossRef]

[2] Paek JS. Analysis and design of low-noise radio-frequency power amplifier supply modulator for frequency division duplex cellular systems. Electronics 2024;13:4635. [CrossRef]

[3] Bowick C, Blyler J, Ajluni C. RF circuit design. 2nd ed. Newnes; 2008.

[4] Pekau H, Haslett JW. Cascaded noise figure calculations for radio receiver circuits with noise-aliasing properties. IET Circuits Devices Syst 2007;1:517–524. [CrossRef]

[5] Pozar DM. Microwave engineering. 2nd ed. John Wiley & Sons; 1998.

[6] Lenka MK, Agrawal A, Khatri V, Banerjee G. A wideband receiver front-end with programmable frequency selective input matching. In: Proc 29th Int Conf VLSI Des 15th Int Conf Embed Syst; 2016; Kolkata, India. p. 168–173. [CrossRef]

[7] Garcia-Vazquez H, Khemchandani SL, Dualibe C, del Pino J. A selectable bandwidth LNA based on current conveyors. In: Proc Argent Sch Micro-Nanoelectron Technol Appl; 2015; Villa Maria, Argentina. p. 33–36. [CrossRef]

[8] Bagga S, Mansano AL, Serdjin WA, Long JR, Philips K, Pekarik JJ. A frequency-selective nested dual-loop broadband low noise amplifier in 90 nm CMOS. In: Proc Eur Solid-State Circuits Conf; 2012; Bordeaux, France. p. 121–124. [CrossRef]

[9] Fernandes M, Oliveira LB, Oliveira JP. A widely tunable narrowband balun-LNA with integrated filtering. In: Proc Int Conf Mix Des Integr Circuits Syst; 2014; Lublin, Poland. p. 160–165. [CrossRef]

[10] Lee J, Han S, Lee J, Kang B, Bae J, Jang J, et al. A sub-6GHz 5G new radio RF transceiver supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL in 14nm FinFET CMOS. In: Proc IEEE Int Solid-State Circuits Conf; 2019; San Francisco, CA, USA. p. 354–356. [CrossRef]

[11] Yeh EHV, Lo AH, Chen WS, Yeh TJ, Chen M. A 16 nm FinFET 0.4 V inductor-less cellular receiver front-end

with ultra-low power and ultra-small area for 5G system in sub-6 GHz band. In: Proc Symp VLSI Circuits; 2017; Kyoto, Japan. p. C72–C73. [CrossRef]

[12] Verma AK, Kumar S. Resistive feedback low noise amplifier for software defined radio. In: Proc Int Conf Green Eng Technol; 2016; Coimbatore, India. p. 1–6. [CrossRef]

[13] Kanth MS, Shanthala S, Raj CP. Performance analysis of inductive source degeneration low noise amplifier using multi-finger technique. Int J Innov Technol Explor Eng 2019;8:1636–1642. [CrossRef]

[14] Sedra AS, Smith KC. Microelectronic circuits. 7th ed. Oxford University Press; 2014.

[15] Razavi B. Design of analog CMOS integrated circuits. 2nd ed. McGraw Hill; 2020.

[16] Han K, Han JH, Je M, Shin H. RF characteristics of 0.18-μm CMOS transistors. J Korean Phys Soc 2002;40:45–48.

[17] Sehmi S, Haddad F, Ben Hammadi A. Impact of multifinger MOSFET geometry on the electrical performance of RF circuits. Microelectron Reliab 2022;129:114445. [CrossRef]

[18] Razavi B. RF microelectronics. 2nd ed. Hoboken, New Jersey: Prentice Hall; 2011.

[19] Huang XH, Chen LJ, Zhou JF, Chen KS. Miller effect analysis and noise optimization of CMOS low noise amplifier. J Zhejiang Univ Sci C 2011;12:424–428.

[20] Tiwat P, Tingting Y, Guoguo L, Xiaojuan C, Xinyu L. MIM series capacitor model for MMIC design application. In: Proc Int Workshop Microw Millim Wave Circuits Syst Technol; 2013; Chengdu, China. p. 475–478. [CrossRef]

[21] Norhapizin K, Ismail MA, Ismat ARA, Marzuki A, Yahya MR, Awang Mat AF. Parasitic effects of spiral inductors on the performance of GaAs-based MMIC low noise amplifier. In: Proc IEEE Int Conf Semicond Electron; 2008; Johor Bahru, Malaysia. p. 134–137. [CrossRef]

[22] Ye F, Chiang JS, Chen CW, Sung YC. Dynamic bias circuits for efficiency improvement of RF power amplifier. In: Proc IEEE Asia-Pac Conf Circuits Syst; 2004. p. 821–824.

[23] Gonzalez G. Microwave transistor amplifiers: Analysis and design. 2nd ed. Hoboken, New Jersey: Prentice Hall; 1997.

[24] Babu DS, Reddy MM, Ramesh G, Babu DS, Daula SMS, Khan GA. A 2.4 GHz LNA design for 802.11 WLAN applications. In: Proc Conf Inf Commun Technol; 2021; Kurnool, India. p. 1–5. [CrossRef]

[25] Kushwaha DS, Rai AK, Agrawal S, Pal PK, Singhal HK. A narrow band cascode source degeneration low noise amplifier with pi-input matching at 5 GHz frequency. In: Proc Int Conf Innov Electron Signal Process Commun; 2019; Shillong, India. p. 301–304. [CrossRef]

[26] Jaradat RO, Shahroury FR, Ahmad HH, Abuishmais I. Design methodology for narrow-band low noise amplifier using CMOS 0.18 μm technology. Jordan J Comput Inf Technol 2022;8:98–111. [CrossRef]

[27] Chou JX, Lin YS. A compact 2.45/5.5-GHz dual-band LNA design using bridged-T coils. In: Proc IEEE Radio Wireless Symp; 2024; San Antonio, TX, USA. p. 115–117. [CrossRef]

[28] Goel R, Kumar A, Kumar M, Kumar S. Design of 1–7 GHz high gain wideband filter LNA for wireless applications. In: Proc Global Conf Adv Technol; 2022; Bangalore, India. p. 1–5. [CrossRef]

[29] Kim MS, Yoo SS. RF-SOI low-noise amplifier using RC feedback and series inductive-peaking techniques for 5G new radio application. Sensors 2023;23:5808. [CrossRef]

[30] Vanukuru V, Ghosal K, Godavarthi N, Dutta A, Narasimhamoorthy S, Swaminathan B, et al. A 6 GHz 0.92 dB NF cascode LNA in 180 nm SOI CMOS technology. In: Proc IEEE MTT-S Int Microw RF Conf; 2019; Mumbai, India. p. 1–4. [CrossRef]

[31] El Meligy AO, Albasha L. Design and analysis of various narrow-band LNA topologies. In: Proc Int Conf Commun Signal Process Their Appl; 2022; Cairo, Egypt. p. 1–7. [CrossRef]

[32] Joshi K, Mandal MK, Mandal P. Design of a wideband differential LNA based in CMOS 180 nm technology. In: Proc IEEE MTT-S Int Microw RF Conf; 2021; Kanpur, India. p. 1–4. [CrossRef]

[33] Abounemra AME, Helaoui M, Ghannouchi FM. A highly survivable C-band GaN HEMT LNA with resistive feedback technique. In: Proc Mediterr Microw Symp; 2019; Hammamet, Tunisia. p. 1–4. [CrossRef]

[34] Wang Z, Li Z, Li J, Wang X, Li Z. A 2.4–5.25 GHz balun-LNA in 22 nm CMOS technology. In: Proc Int Conf Integr Circuits Microsyst; 2021; Nanjing, China. p. 197–200. [CrossRef]

[35] Wang J, Wen J, Chi PL, Yang T. A 2.8–3.8 GHz reconfigurable GaAs low-noise amplifier with improved blocker tolerance. IEEE Microw Wireless Technol Lett 2024;34:419–422. [CrossRef]