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Research Article

Overview of single-phase-shift dual active bridge converter: operation, analysis, design guidelines and comparison of optimized control strategies

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ABSTRACT

This paper discusses the operation, design guidelines, and control strategies of the bidirectional dual-active bridge (DAB) converter with single-phase-shift (SPS) modulation. Some key issues, such as steady-state analysis, average values, output voltage ripples, and soft-switching operations, are also addressed in detail. The operation modes are individually investigated for heavy and light load conditions, and the boundary load conditions that will maintain the converter in the soft-switching region are derived. The output ripple analysis is conducted only under heavy load conditions for each operation mode. Some practical considerations are presented for design procedures. The transformer turn ratio trade-offs are discussed to configure the zero-voltage switching (ZVS) operating range as well as characterize the root-mean-square (RMS) current level. Simple design guidelines are proposed for the best design that allows the converter to operate in the ZVS region as much as possible in case of a wide input voltage range. This study further discusses five different PI-based control strategies, namely traditional voltage loop control, load current feedforward control, enhanced model-based phase-shift control, basic direct power control, and virtual direct power control. To be used in simulation studies, an exemplary converter with 50W rated power that steps down the input voltage of between 36V and 60V to 5V is designed. All theoretical analyses are confirmed by the simulation results of the designed converter. Similarly, the control strategies are tested for three different operating scenarios through the designed converter. The results are evaluated in terms of the transient and steady-state responses. A comparative analysis of control strategies is presented, and the scheme that exhibits the best performance is determined.

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INTRODUCTION

The dual-active bridge (DAB) converter was first introduced in the early 1990s [1]. Nowadays, it has become an indispensable part of most industrial dc-dc power conversion systems. High power density, zero-voltage switching (ZVS), bidirectional power flow, voltage matching, and galvanic isolation are the most important capabilities that make it prominent in the next generation of dc-dc power conversions. Compared to other isolated topologies, DAB converter has now become a very popular topology, especially for distributed generating systems [2-5], energy conversion [6-9], and storage applications [10-13].

The most attractive way to control the DAB converter is to use phase-shift modulation techniques. The first phase-shift modulation was presented when the DAB converter was proposed in [1]. This is called conventional single-phase-shift (SPS) modulation in literature. The performance characteristics of the DAB converter under SPS control are examined in [14]. In this study, the regions of soft-switching for both bridges are identified, and the impacts of parasitic elements on the regions are also discussed. More detailed analyses on the converter are conducted in [15-18]. The paper in [16] details the operation modes of the DAB converter with SPS control according to load conditions (light and heavy load) and derives the mathematical expressions for each possible operation modes. Some key analyses are also made on voltage ripple, deadband effect, and safe operating area (SOA). In [19], several practical considerations, such as switches capacitance, dead time, series inductance design, and input/output voltage variation, are considered to fully analyze the ZVS range of the converter. Different purpose design strategies and techniques to improve the performance of the DAB converter with SPS control are presented in [20]. The study proposes two different design approaches to increase the soft-switching operation range and to improve efficiency at full load. Moreover, some modifications that can be made to improve the performance of the converter are also mentioned. Using the SPS modulation method, it is quite difficult to remain the converter in the ZVS region at different voltage conversion ratios over the entire power range. The ZVS range of the converter will narrow as the voltage conversion ratio moves away from unity and will even disappear completely for light load conditions. Moreover, power flow control is dependent on the leakage inductance of the transformer, leading to high-circulating power when the voltages on both sides of the transformer are mismatched [21,22]. This causes both root-mean-square (RMS) and peak currents to increase. The above troubles boost power losses and adversely affect the efficiency of the converter. In recent years, to tackle these challenges and improve converter efficiency, some typical phase-shift modulation methods, such as Dual-Phase-Shift (DPS) modulation [23], extended-phase-shift (EPS) modulation [2,24], and triple-phase-shift (TPS) modulation [25] have been proposed. Compared with the SPS modulation, these include multiple modulation parameters, which increase the degree of freedom in the control. The TPS modulation is general since it has three control freedoms, and the DPS and EPS modulations with two degrees of freedom are considered as the special cases of that [22]. Multiple degrees of freedom allow the converter to reduce the current stress, extend the ZVS operating range, and decrease the reactive (backflow) power [21,22,26]. Therefore, the TPS modulation can typically exhibit better performance in power efficiency than others [22,26]. The necessity to determine multiple modulation parameters brings several difficulties in their analysis and control process. To this end, many efficiency optimization strategies are combined with the DPS, EPS, and TPS techniques to determine the modulation parameters. The optimal modulation schemes recently introduced have made the converter operate with minimized RMS current [27-29], reduced conduction losses [30] and power losses [24,31-33], decreased current stress [34-36], and minimized reactive power [23,37]. Moreover, some of these studies have combined soft switching optimization with RMS current minimization [27,28] and reactive power reduction [37] to extend the ZVS operation range. However, all these schemes suffer from complex calculations and a high computational burden. This means that real-time implementations will become quite challenging, especially for the TPS modulation. As a way to solve the realization difficulty, most schemes [26,28,31] utilize lookup tables (LUTs) which store the modulation parameters optimized in advance under different operating conditions. To extract the modulation variables in practice, the current operating conditions are first detected, and then these LUTs are searched. This situation results in low accuracy and unsatisfactory modulation performance due to the inherent discrete outputs of LUTs [33,34]. As another solution, some researchers have developed artificial intelligence-based approaches, such as neural network and fuzzy inference system [33,34], deep reinforcement learning [32], data-driven [36] and augmented Lagrangian method [37]. Such techniques enable online calculations in determining the optimum modulation variables and come to the fore in the context of low computation and automating the control process. Despite the benefits of more than one degree of freedom offered by DPS, EPS, and TPS modulation techniques, SPS modulation still remains relevant, especially for applications that prioritize simplicity and cost-effectiveness. The rationale underlying this claim can be expressed as the modulation process being less complex and easier to implement.

The most primitive and traditional methods for the control of the DAB converter are single-loop voltage or current feedback control schemes. Voltage mode control is used to regulate the output voltage in case of unidirectional power flow. Current mode control is preferred to regulate bidirectional power flow between two sources. The dynamic performance of both two traditional methods under load

changes is quite poor. Therefore, this situation has caused many researchers to focus on advanced control schemes to enhance the dynamic response and static performance of the converter. In [38], to increase the stability margin of voltage mode control, a linearized control method has been proposed. In this control, unlike the traditional scheme, a linearization operator is used. Thus, by eliminating or compensating the nonlinear terms between the output current and the phase shift ratio, the sensitivity of the stability of the voltage mode control to the load condition is reduced. The voltage mode control has also been improved by using an inner current loop in addition to the outer voltage loop. This is also called average current control (ACC), and it is generally used to control the current in any circuit branch [39]. In this scheme, when the output current is fed back, not only the output power can be directly controlled but also overcurrent protection can be provided. However, in some studies, the feedback current for the DAB converter is also taken as the secondary side bridge current [40,41], the output load current [41], the active component of the transformer leakage inductance current [42], or the output LC filter current [43,44]. The two-closed loop control, like voltage mode control, exhibits slow transient responses during load changes. The reason for this is clarified as a result of the analyses made in [41] and it is stated that it is due to the high closed-loop output impedance. Load current feedforward (LCFF) controls have been proposed in [40,41,45] to reduce the closed-loop output impedance and thus accelerate the load step response. As an alternative to voltage mode control, a model-based phase shift (MPS) control has been presented in [46,47] for the converter feeding a resistive load. The MPS control is based on directly calculating the desired phase-shift ratio, and thus it requires both estimating the load resistance online and measuring the load current and input voltage accurately. In general, it is quite sensitive to the converter parameters and exhibits relatively poor dynamic responses to load changes. To improve the overall performance of the MPS control, a PI controller has been adapted to this scheme [47], and it was called enhanced-MPS (e-MPS) control. Recently, direct power (DP) control, which is widely used in renewable generation systems, is emerging as an effective method to achieve robust dynamic response. In the DAB converters, the DP control has been developed in different ways using the relationship between the transferred power and the phase shift ratio. The common goal is to ensure that the converter reaches the desired output power quickly. Basic DP control is presented in [48,49] for the DAB converter. As in the e-MPS control, the basic scheme is dependent on the converter parameters, and it is also necessary to feed forward the load current and input voltage precisely. A different approach to DP control is proposed in [50]. In this method, defined as virtual DP (VDP), the necessity of using converter parameters to calculate the desired phase shift ratio is eliminated, but it still requires feedforward. All the control schemes outlined above use traditional PI controllers to deal with input voltage fluctuations and load variations. Thus, this study has referred to them as PI-based control schemes. In recent years, superior control strategies to PI-based control schemes have also been proposed, such as model predictive control [51-53], sliding mode approaches [54-56], and disturbance observer-based control [57-59]. These advanced control methods are more robust to disturbances in input voltage and load variation, model uncertainty, and circuit parameter variations when compared to PI-based schemes. However, they are quite complex to implement and require a small signal model of the converter for their design. A comprehensive review of advanced control methods is presented in [60]. This study discusses five different control strategies based on conventional PI controller. The reasons for focusing on PI-based control schemes are as follows: (i) their implementation cost and complexity are low, (ii) they do not require a small signal model of the converter for their design, (iii) they are widely used since they can be easily designed in the time domain, (iv) controller parameters can be adjusted by the trial-and-error method, and also metaheuristic optimization algorithms are easy to apply in parameter tuning.

The main contributions of this paper are:

(i) A comprehensive analysis is presented for the DAB converter with SPS control. This study has a complementary nature to previous studies.
(ii) Some practical considerations are discussed regarding design procedures. Based on the turn ratio tradeoffs, a simple guide is proposed to the designers for their design, especially in a wide input voltage range. It allows the converter to operate in the ZVS region as much as possible over a wide power range.
(iii) This study comprehensively discusses five different PI-based control strategies. A detailed comparative analysis on the transient and steady-state responses of these strategies is presented, and the control scheme that gives the best dynamic and static performance is determined.

The paper is organized into six sections. In Section 2, the basic operation principle of the DAB converter is briefly examined. Besides, the steady-state analysis of the converter is carried out, and some mathematical derivations are made on the average values, output voltage, and output voltage ripple. At the end of this section, the regions of soft-switching for both bridges are shortly discussed. Some practical design considerations and guidelines are given in Section 3. In Section 4, PI-based control strategies are explained in detail. The simulation results are given in Section 5, and the drawn conclusions are evaluated in Section 6.

DUAL-ACTIVE BRIDGE CONVERTER

Basic Operation Principle

The simplified circuit diagram of a single-phase DAB converter is shown in Figure 1(a). It typically consists of two full bridges interfaced through a high-frequency

transformer. The inductor L is usually defined as the sum of the auxiliary inductor in series with the transformer and the leakage inductance of the transformer itself. The transformer allows a high voltage conversion ratio when its turn ratio is set appropriately, as well as providing galvanic isolation. The power flow between two full bridges is bidirectional in the presence of an active load, and conceptually, it is similar to the power transmission in a traditional AC power system. This analogy is depicted in Figure 1(b), where all quantities are referred to the primary side.

Fundamentally, the DAB converter can be easily controlled using conventional SPS modulation. In this scheme, there is a certain phase-shift between the gate signals of two bridges, and all switches operate at constant pulse width with a 50% duty cycle. Figure 2 illustrates the basic theoretical waveforms of the converter for the main operation mode ($V_1 = NV_2$) under SPS control. As seen in Figure 2, the primary and secondary voltages of the transformer are high-frequency square waves, which are out of phase, and the primary voltage is in leading phase relative to the secondary one. Therefore, power is delivered from the primary side bridge towards the other, which is referred to as forward power flow. The direction of power flow and magnitude can be controlled by adjusting the sign and value of the phase-shift between two bridges properly.

The DAB converter can further operate in two distinct modes other than main operating mode. In general, these are defined based on the following voltage conversion ratio:

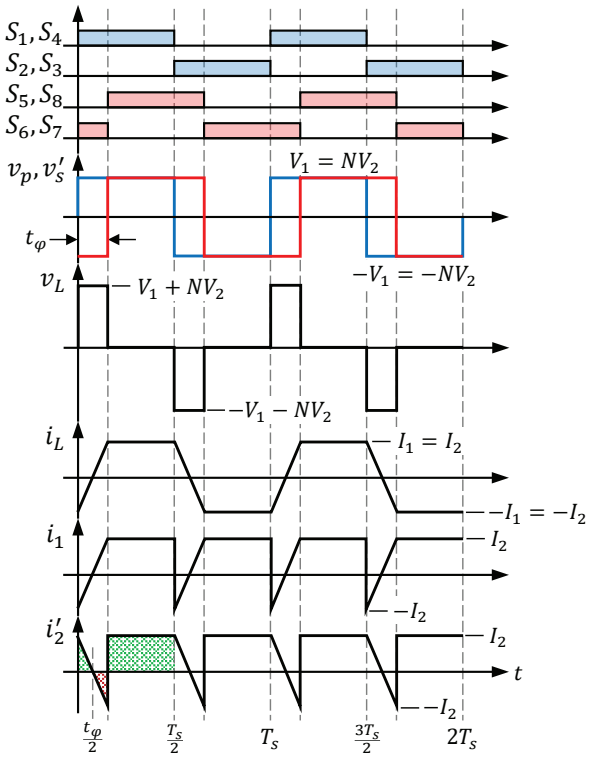

Figure 2. Basic theoretical waveforms for main operation mode ($V_1 = NV_2$) under SPS control, where $T_s = 1/f_s$ and f_s is the switching frequency.

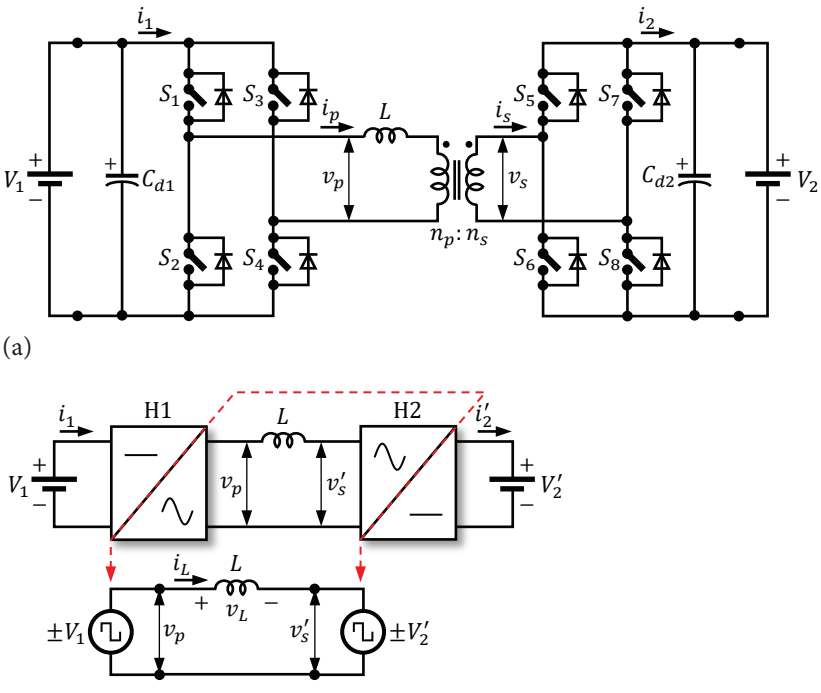

Figure 1. (a) Simplified circuit diagram of the DAB converter. **(b)** Equivalent schematic of the DAB converter with phase-shift control. ($N = n_p/n_s$ is the turn ratio of the transformer, and v_s', i_s' are quantities reduced to the primary side.).

$$m = \frac{NV_2}{V_1} \tag{1}$$

where $m < 1$, $m = 1$, and $m > 1$ represent buck ($V_1 > NV_2$), main ($V_1 = NV_2$), and boost ($V_1 < NV_2$) operation modes, respectively. Similar theoretical waveforms for $m < 1$ and $m > 1$ are presented in detail under different load conditions in Figure 3 and Figure 4. It is seen that the inductor current for m = 1 is always trapezoidal regardless of load conditions, and yet it varies with light and heavy load conditions for $m < 1$ and $m > 1$. The analysis of the inductor current is quite significant in obtaining some important mathematical derivations, and it will be discussed in more detail for all possible operating modes by performing the steady-state analysis in the next subsection.

Steady-State Analysis

To simplify the steady-state analysis, the following assumptions are made: (i) the winding resistances and magnetizing inductance of the transformer are neglected, (ii) all semiconductor devices are ideal, that is the parasitic and snubber capacitance are ignored, (iii) the dead-time effect and switching dynamics are neglected, (iv) all quantities are addressed to the primary side of the transformer. Under these assumptions, four different segments in the inductor current occur during

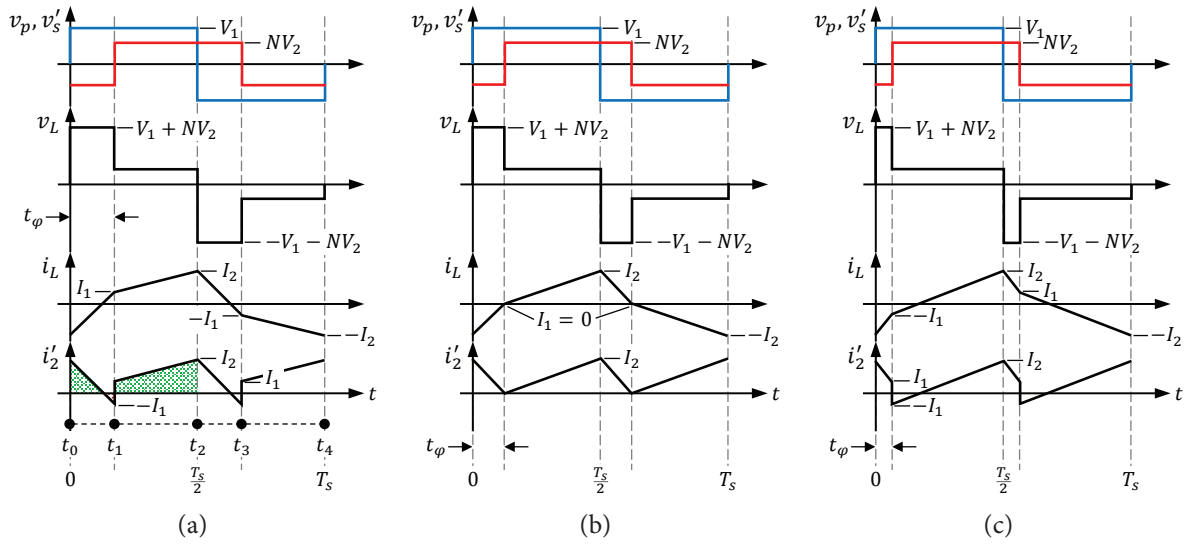

Figure 3. Basic theoretical waveforms for buck operation mode ($V_1 > NV_2$ or $m < 1$) under **(a)** heavy, **(b)** boundary, and **(c)** light load conditions.

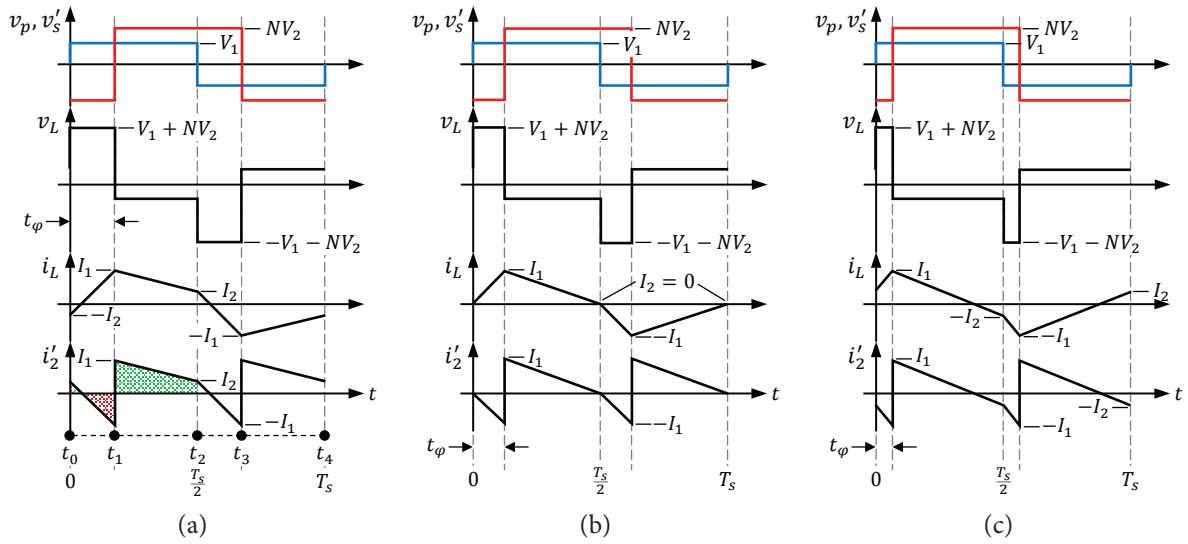

Figure 4. Basic theoretical waveforms for boost operation mode ($V_1 < NV_2$ or $m > 1$) under **(a)** heavy, **(b)** boundary, and **(c)** light load conditions.

only one switching period, as shown in Figure 2, Figure 3, and Figure 4. In each segment, the difference between the primary and secondary voltages of the transformer appears across the inductor, and since $\frac{di_L}{dt} \approx \frac{\Delta i_L}{\Delta t}$ for $\Delta t \to 0$, the slope of the inductor current can be approximated by

$$\frac{\Delta i_L}{\Delta t} \approx \frac{v_L}{L} \tag{2}$$

where Δi_L is the change of the current in the related segment and Δt is the time interval of this segment. With this approach, the change in inductor current is assumed to be linear over the interval Δt. Consequently, when only concerning the waveforms in Figure 3(a), the inductor current analysis is realized as follows:

Segment 1 [t_0, t_1]: The inductor current increases from a negative initial value $i_L(t_0) < 0$ to a positive value $i_L(t_1) > 0$ throughout this segment. The time interval is equal to $\Delta t = t_\varphi$, and also the voltage across the inductor is $v_L = V_1 + NV_2$. Hence, the inductor current increment Δi_L is defined from Eq. (2) as

$$i_L(t_1) - i_L(t_0) = t_\varphi \left(\frac{V_1 + NV_2}{L}\right) \tag{3}$$

where i_L (t_0) and i_L (t_1) are the inductor current values at the instant of t_0 and t_1, respectively. t_φ is the phase-shift in times. $t_\varphi = \frac{\phi}{2\pi f_s}$ and ϕ is the phase-shift angle, $0 < \phi < \pi/2$.

Segment 2 [t_1, t_2]: The inductor current continues to increase linearly during this segment up to a positive peak value $i_L(t_2) > 0$, where $\Delta t = \frac{T_s}{2} - t_\varphi$. Since the inductor voltage is $v_L = V_1 + NV_2$, the current increment is

$$i_L(t_2) - i_L(t_1) = \left(\frac{T_s}{2} - t_\varphi\right)\left(\frac{V_1 - NV_2}{L}\right) \tag{4}$$

where $i_L(t_2)$ is the inductor current value at the instant of t_2. $T_s = 1/f_s$ and f_s is the switching frequency.

Segment 3 [t_2, t_3] and 4 [t_3, t_4]: Due to the half-wave symmetry of the operation, it is sufficient to deduce the equations of the inductor current for only a half cycle. However, using a similar analysis to the one described in the previous two segments (1 and 2), these can be obtained for the remaining segments (3 and 4) as

$$i_L(t_3) - i_L(t_2) = -t_\varphi \left(\frac{V_1 + NV_2}{L}\right) \tag{5}$$

$$i_L(t_4) - i_L(t_3) = -\left(\frac{T_s}{2} - t_\varphi\right)\left(\frac{V_1 - NV_2}{L}\right) \tag{6}$$

where i_L (t_3) and i_L (t_4) are the inductor current values at the instant of t_3 and t_4, respectively. On the other hand, given the symmetrical waveform of the current, the following definitions are made:

$$\begin{aligned} i_L(t_1) &= -i_L(t_3) = I_1 \\ -i_L(t_0) &= i_L(t_2) = -i_L(t_4) = I_2 \end{aligned} \tag{7}$$

where I_1 and I_2 are the instantaneous values of the inductor current the instant that two full bridges are switched. After some algebraic manipulations using Eqs. (3), (4), and (7), I_1 and I_2 can be obtained as

$$I_1 = \frac{1}{4f_sL}(NV_2 - (1-2d)V_1) \tag{8}$$

$$I_2 = \frac{1}{4f_sL}(V_1 - (1-2d)NV_2) \tag{9}$$

where $d = \phi / \pi$ is the phase-shift ratio.

Main Operation Mode ($m = 1$): As seen in Figure 2, the two instantaneous values of the inductor current are equal to each other, $I_1 = I_2$. Thus, since $V_1 = NV_2$ for this mode, this can be calculated using Eq. (8) or (9) as

$$I_1 = I_2 = \frac{V_1}{2f_sL}d \tag{10}$$

Buck Operation Mode ($m < 1$): In this mode, as deduced from Figure 3, the relationship between the two instantaneous values of the inductor current can be written as $I_2 > I_1$. Depending on the load conditions or the average transferred power, I_2 is always a negative value at the beginning of the switching cycle, but I_1 can be a positive or negative value at the end of the first segment; $I_1 > 0$ and $I_1 < 0$ for heavy and light loads, respectively. The boundary load condition results when $I_1 = 0$. Hence, considering Eq. (8) with $I_1 = 0$, we obtain

$$\phi_{buck} = \frac{\pi}{2}(1-m) \tag{11}$$

where ϕ_{buck} is the phase-shift angle for the boundary load condition of buck mode. Besides, by substituting Eq. (11) into Eq. (9), the instantaneous value I_2 in Figure 3(b) can be calculated as

$$I_2 = \frac{V_1}{4f_sL}(1-m^2) \tag{12}$$

Table 1. Phase-shift angles depending on the load conditions for each operation mode

	Load Conditions		
Operation Mode	**Heavy**	**Boundary**	**Light**
Buck ($m < 1$)	$\phi > \phi_{buck}$	$\phi = \phi_{buck}$	$\phi < \phi_{buck}$
Boost ($m > 1$)	$\phi > \phi_{boost}$	$\phi = \phi_{boost}$	$\phi < \phi_{boost}$

It is noted that Eq. (12) holds for only the boundary phase-shift angle, $\phi = \phi_{buck}$. Eqs. (8) and (9) still represent I_1 and I_2 for other conditions, $\phi > \phi_{buck}$ and $\phi < \phi_{buck}$.

Boost Operation Mode ($m > 1$): Similar definitions above could be performed for the boost operation mode. As given in Figure 4, the difference is that the relationship is $I_1 > I_2$, and I_2 emerges as $I_2 < 0$ and $I_2 > 0$ at the beginning of the switching cycle under heavy and light loads, respectively. The boundary load condition occurs this time for $I_2 = 0$. Hence, considering Eq. (9) with $I_2 = 0$, we obtain

$$\phi_{boost} = \frac{\pi}{2}\left(1 - \frac{1}{m}\right) \tag{13}$$

where ϕ_{boost} is the phase-shift angle for the boundary load condition of boost mode. In addition, the substitution of Eq. (13) into Eq. (8) results in

$$I_1 = \frac{V_1}{4f_sL}\left(m - \frac{1}{m}\right) \tag{14}$$

It is noted that Eq. (14) holds for only the boundary phase-shift angle, $\phi = \phi_{boost}$. Eqs. (8) and (9) still represent I_1 and I_2 for other conditions, $\phi > \phi_{boost}$ and $\phi < \phi_{boost}$. Table 1 summarizes the phase-shift angles depending on the load conditions for each operation mode.

Average Values

The output current of the secondary side bridge is a rectified version of the inductor current, as shown in Figure 2. Due to the symmetry of the inductor current, the average output current is derived for a semi-period as

$$\bar{I}_2' = \frac{2}{T_s}\int_0^{T_s/2} i_2'(t)\,dt = \frac{2}{T_s}A_{shaded} \tag{15}$$

where $\bar{I}_2'$ denotes the average of the output current, and A_{shaded} is the sum of the shaded areas given in Figure 2. Then, A_{shaded} can be calculated by

$$A_{shaded} = I_2\left(\frac{T_s}{2} - t_\varphi\right) \tag{16}$$

and substituting Eq. (10) into Eq. (16), the average output current $\bar{I}_2'$ is

$$\bar{I}_2' = \frac{V_1}{2f_sL}d(1-d) \tag{17}$$

Hence, the average output power is

$$P_2 = V_2'\bar{I}_2' = \frac{NV_1V_2}{2f_sL}d(1-d) \tag{18}$$

On the other hand, assuming all losses are neglected, the average supplied power is equal to the output power, that is $P_1 = P_2$ or $V_1\,\bar{I}_1' = V_2'\,\bar{I}_2'$. Then, the average supplied current $\bar{I}_1'$ is obtained as

$$\bar{I}_1 = \frac{P_2}{V_1} = \frac{NV_2}{2f_sL}d(1-d) \tag{19}$$

The above analysis was performed for the main operation mode ($m = 1$). The given average expressions can also be reached on the basis of the waveform of i_2' for the buck ($m < 1$) or boost ($m > 1$) modes. The shaded areas in Figure 3(a) and Figure 4(a) constitute the data used to obtain the same average values.

The average expressions in Eqs. (17), (18), and (19) are actually for forward power flow. For both power flows, the unified expressions can be rearranged as follows:

$$P_1 = P_2 = \frac{V_1^2}{X_L}m\phi\left(1 - \frac{|\phi|}{\pi}\right) \tag{20}$$

$$\bar{I}_1 = \frac{V_1}{X_L}m\phi\left(1 - \frac{|\phi|}{\pi}\right) \tag{21}$$

$$\bar{I}_2' = \frac{NV_2}{X_L}\frac{\phi}{m}\left(1 - \frac{|\phi|}{\pi}\right) \tag{22}$$

where $X_L = 2\pi f_sL$ and the phase-shift angle is $0 < \phi < \pi/2$ and $-\pi/2 < \phi < 0$ for forward and backward (reverse) power flow. Figure 5 illustrates the characteristic curves of output power versus phase-shift angle for bidirectional power flow, where the voltage conversion ratio m was taken as a variable parameter. This shows that the output power and $d = \phi / \pi$ have a parabolic relationship, and accordingly, the nonlinearity of the output power will be more severe with an increasing value of d. The region of soft-switching for both bridges is also identified in Figure 5. For $m = 1$, the output power characteristic is enclosed by the soft-switching boundaries, and thus all devices can be operated under soft-switching in the full range of d. However, the control range is narrowed in the buck or boost operations, and

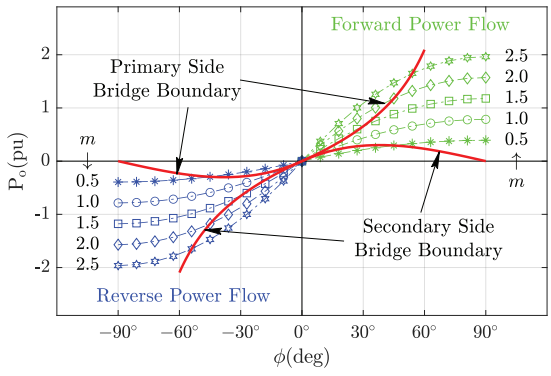

Figure 5. Characteristic curves of output power versus phase-shift angle for different voltage conversion ratios.

hard-switching may occur in some load conditions. The soft-switching region of operation of the DAB converter will be discussed in detail later.

Output Voltage

To express the output or load voltage, let us assume a simple schematic of the converter given in Figure 6(a), where a load resistor R_L is attached to the output of the secondary side bridge instead of an active load. Unlike Figure 1, the operation is now unidirectional, and the power flow is from the source to the passive load. In this circumstance, the output power for a fixed resistive load is defined as

$$P_2 = \frac{V_o^2}{R_L} \tag{23}$$

and combining with Eq. (18), the load voltage can be expressed as

$$V_o = \frac{NV_1}{2f_sL} R_L d(1-d) \tag{24}$$

where V_o is the load voltage, and it can be considered constant at steady-state when the output filter capacitor is chosen large enough to provide significant filtering of the switching ripples. Eq. (24) indicates that, for a particular f_s, L, and V_1, the output voltage is proportional to R_L and has a parabolic relationship with d. Therefore, for a given R_L, the output voltage reaches its maximum value when d = 0.5. Also, for a given d, the operating modes directly depend on the value of R_L, and the main operation mode occurs when R_L is equal to its boundary value. Using Eq. (24), the boundary load resistance for NV_o= V_1 (m = 1) can be calculated by

$$R_{bound} = \frac{2f_sL}{N^2} \frac{1}{d(1-d)} \tag{25}$$

where 0 < d < 0.5. Under heavy load conditions for $d > \phi_{buck} / \pi$, when $R_L < R_{bound}$, the buck operation occurs. Otherwise, the boost operation arises from R_L>R_{bound}, in which $d > \phi_{boost} / \pi$ for heavy loads. As shown in Figure 6(a), the load current is $i_o = i_2 - i_C$. Assuming the peak-to-peak current ripple ΔI_o is small enough to be neglected, then it means $\Delta I_2 = \Delta I_C$. Thus, the load current is also considered constant, and $I_o = N\bar{I}_2'$ or $I_o = V_o/R_L$. From Eq. (17) or (24), the load current is obtained as

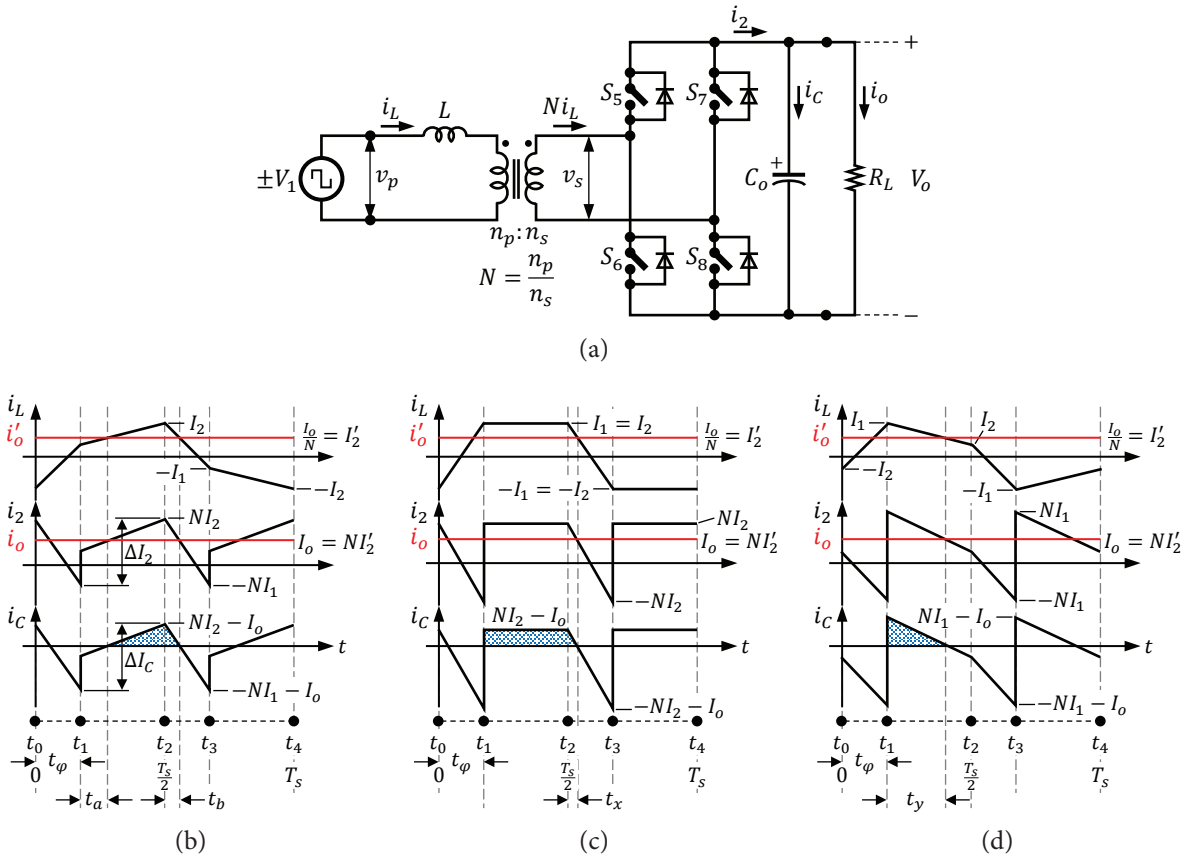

Figure 6. (a) Simplified circuit diagram used for load voltage and output ripple analysis. Current ripple in the output capacitor for **(b)** Buck (m < 1, $\phi > \phi_{buck}$), **(c)** Main (m = 1), and **(d)** Boost (m > 1, $\phi > \phi_{boost}$) operation modes, where i'_o is load current reduced to the primary side.

$$I_o = \frac{NV_1}{2f_sL} d(1-d) \tag{26}$$

The load current I_o along with the output current i_2 of the secondary side bridge and the capacitor current i_C for each operation mode are shown in Figure 6(b), Figure 6(c), and Figure 6(d). Here, the output waveforms only for heavy load conditions are discussed.

Voltage Ripple Analysis

All switched-mode power supplies have an inherent switching phenomenon, which causes an undesired ripple in the load voltage. Generally, the voltage ripple is directly proportional to the total charge accumulated (or discharged) across the output filter capacitor. The total charge corresponds to one of the positive or negative areas of the capacitor current in Figure 6.

For buck operation mode ($m < 1$), the voltage ripple is defined as

$$\Delta V_{o,buck} = \frac{1}{C_o} \int_{t_\varphi + t_a}^{\frac{T_s}{2}+t_b} i_C(t)\, dt = \frac{1}{C_o} \Delta Q_{buck} \tag{27}$$

where $\Delta V_{o,buck}$ is the peak-to-peak voltage ripple, and ΔQ_{buck} is the total charge accumulated across C_o. Considering the shaded areas in Figure 6(b), ΔQ_{buck} can be calculated by

$$\Delta Q_{buck} = \frac{1}{2}(NI_2 - I_o)\left(\frac{T_s}{2} - t_\varphi - t_a\right) + \frac{1}{2}(NI_2 - I_o)t_b \tag{28}$$

where t_a and t_b are derived from Eqs. (4) and (5) as

$$t_a = \frac{L}{N(NV_o - V_1)}(NI_1 - I_o) \tag{29}$$

$$t_b = \frac{L}{N(NV_o + V_1)}(NI_2 - I_o) \tag{30}$$

and also, from Eqs. (8), (9), and (26), we obtain

$$NI_1 - I_o = \frac{N}{2f_sL}\left(d^2V_1 - \frac{1}{2}(V_1 - NV_o)\right) \tag{31}$$

$$NI_2 - I_o = \frac{N}{2f_sL}\left(\left(\frac{1}{2} - d\right)(V_1 - NV_o) + d^2V_1\right) \tag{32}$$

Eventually, the rearrangement of Eq. (28) using the last equalities yields

$$\Delta Q_{buck} = \frac{N}{8f_s^2L}\left(\Delta_1(V_1 - NV_o) + \Delta_2 V_1 + \frac{\Delta_3}{V_1 + NV_o}\right) \tag{33}$$

where

$$\Delta_1 = \frac{1}{4} - d + d^2$$

$$\Delta_2 = d^2\left(1 - 2d + \frac{V_1}{V_1 - NV_o}d^2\right)$$

$$\Delta_3 = \left(\left(\frac{1}{2} - d\right)(V_1 - NV_o) + V_1 d^2\right)^2$$

Similarly, the ripple analysis for the other two operation modes should also be carried out individually because the total charge contained across C_o is different in each mode. In this context, using the shaded areas in Figure 6(c) and Figure 6(d), the total charges are obtained as

$$\Delta Q_{main} = \frac{NV_1}{4f_s^2L} d^2\left(1 - d + \frac{1}{4}d^2\right) \tag{34}$$

$$\Delta Q_{boost} = \frac{N}{8f_s^2L}\frac{1}{NV_o - V_1}\left(\frac{1}{2}(NV_o - V_1) + V_1 d^2\right)^2 \tag{35}$$

Then, the peak-to-peak voltage ripples for $m = 1$ and $m > 1$ are

$$\Delta V_{o,main} = \frac{1}{C_o}\Delta Q_{main} \tag{36}$$

$$\Delta V_{o,boost} = \frac{1}{C_o}\Delta Q_{boost} \tag{37}$$

The voltage ripple is a significant parameter used to determine the output filter capacitor. In a well-designed converter, the output capacitor is chosen to keep the percentage ripple usually less than 1 - 2%. The percentage ripple is defined as $\Delta V_o(\%) = \frac{\Delta V_o}{V_o} \times 100$, where V_o is the steady-state value of the load voltage. More details on the output capacitor selection will be presented under the Design Guidelines.

Soft Switching Operation

In the DAB converter, the switches on the same leg in both active bridges operate in a complementary manner (see Figure 2). Thus, to prevent a possible short circuit, a dead-time should be implemented during which both switches are turned off. Throughout this dead-time, the output parasitic capacitances of the switches that will be turned from off to on are discharged with the energy stored in the inductor, and the voltages across them drop to zero before they are turned on. The voltage across the switches being zero at the instant of turn-on is known as zero-voltage switching (ZVS). ZVS is a phenomenon that provides soft-switching transients and reduces switching losses. Examining the gate signals in Figure 2, ZVS for the secondary side bridge occurs during the transitions from segment 1 to 2 and segment 3 to 4, while the primary side bridge executes it during other consecutive segments (segment 2 to 3 and segment 4 to 1).

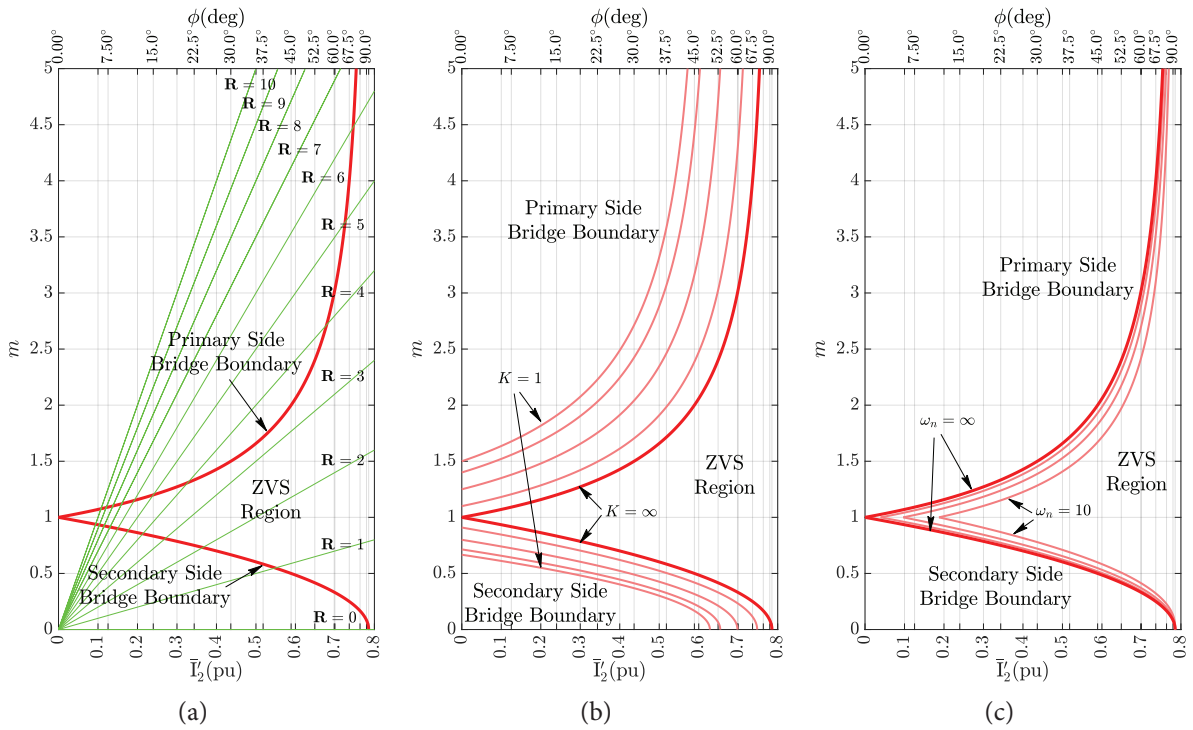

Figure 7. (a) Representation of the ZVS boundaries for the primary and secondary side full bridges. Influences of transformer magnetizing inductance **(b)** and device output capacitances **(c)** on the ZVS region of operation.

As stated earlier, provided that $m = 1$, ZVS is maintained over an entire power range for both full bridges. However, when m is not equal to 1, and as the handled power is reduced (at light loads), the ZVS region narrows gradually. It may even disappear for certain values of m and d. For this reason, when $m < 1$ or $m > 1$, ZVS will be fulfilled only under the heavy load cases discussed previously. As can be easily deduced from Figure 3(a) and Figure 4(a), the ZVS conditions for the primary side bridge are

$$S_1, S_4 : i_L(t_0) < 0, \quad S_2, S_3 : i_L(t_2) > 0$$

while for the secondary side bridge, they are

$$S_5, S_8 : i_L(t_1) > 0, \quad S_6, S_7 : i_L(t_3) < 0$$

Due to the half-wave symmetry of the inductor current, the given conditions can be simplified to $I_2 > 0$ and $I_1 > 0$. From Eqs. (8) and (9), I_1 and I_2 can be rewritten as

$$I_1 = \frac{\pi}{2} I_n (2d - 1 + m) \tag{38}$$

$$I_2 = \frac{\pi}{2} I_n (2md + 1 - m) \tag{39}$$

where $I_n = V_1 / X_L$ is the nominal base current. Hence, using Eqs. (38) and (39), the necessary conditions to ensure ZVS for the primary and secondary side bridges are respectively obtained as

$$\phi > \frac{\pi}{2}\left(1 - \frac{1}{m}\right) \tag{40}$$

$$\phi > \frac{\pi}{2}(1 - m) \tag{41}$$

These two conditions are depicted in Figure 7(a), where the bold curves enclose the region of operation of the DAB converter under ZVS. The x-axis represents the normalized output current and phase-shift angle (with different scales), while the y-axis represents the voltage conversion ratio. From Eq. (17), the normalized output current is given by

$$\bar{I}'_2(\text{pu}) = \frac{\bar{I}'_2}{I_n} = \phi\left(1 - \frac{\phi}{\pi}\right) \tag{42}$$

and

$$\mathbf{R} = \frac{m}{\bar{I}'_2(\text{pu})} \tag{43}$$

where $\mathbf{R}$ is the normalized load line. The intersection of the m and $\mathbf{R}$ lines gives the operating phase-shift angle ϕ. If this operating point is within the ZVS region, then the converter is expected to perform soft-switching. It is also seen from Figure 7(a) that ZVS will be satisfied only for certain values of m and $\bar{I}'_2$, and the operation under ZVS will be more possible with an increasing value of output current (which implies higher power transfer) even if m is quite different from 1.

Some parasitic elements affect the ZVS region of the converter. The parasitic elements that have the most dominant effect are transformer magnetizing inductance and switch output capacitances. The above analysis was performed under the assumption that the magnetizing inductance is infinite and the output capacitances are neglected. Therefore, these ZVS boundaries are ideal curves and cannot always guarantee ZVS operation. An investigation into the influence of the parasitic elements on the ZVS region is presented in [14,20]. Based on these studies, the given conditions in Eqs. (40) and (41) to achieve ZVS in both bridges can be rearranged as

$$\phi > \frac{\pi}{2}\left(1-\left(1+\frac{1}{2K}\right)\frac{1}{m}+\frac{\mathrm{I_{Lmin}(pu)}}{m}\right) \tag{44}$$

$$\phi > \frac{\pi}{2}\left(1-\left(1+\frac{1}{2K}\right)m+\mathrm{I_{Lmin}(pu)}\right) \tag{45}$$

where the transformer magnetizing inductance is defined as $L_m = K \times L$ and $K \geq 1$. I_{Lmin} is the minimum inductor current required to ensure ZVS, that is I_1 and I_2 should always be higher than I_{Lmin}. It is described as

$$I_{Lmin} = 2\sqrt{NV_1V_2}\sqrt{\frac{C_{oss}}{L}}$$

and the normalized I_{Lmin} is

$$\mathrm{I_{Lmin}(pu)} = \frac{I_{Lmin}}{I_n} = \frac{2}{\omega_n}\sqrt{m}\,,\quad \omega_n = \frac{1}{2\pi f_s\sqrt{LC_{oss}}}$$

where C_{oss} is the switch output capacitance. Finally, the normalized output current is now expressed as

$$\bar{\mathrm{I}}_2'\mathrm{(pu)} = \frac{\bar{I}_2'}{I_n} = \left(\frac{4K}{1+4K}\right)\phi\left(1-\frac{\phi}{\pi}\right) \tag{46}$$

Using Eqs. (44), (45), and (46) and for $C_{oss} \approx 0$ or $\omega_n \approx \infty$, the influence of magnetizing inductance on the ZVS region is depicted for different K values in Figure 7(b). The extreme values of L_m are obtained for $K = 1$ and $K = \infty$. It is seen that the ZVS region widens as K decreases. Although the low magnetizing inductance seems to be an advantage, this causes the transformer utilization factor (TUF) to decrease. Nevertheless, K can be used as a trade-off mechanism to achieve efficient voltage conversion, especially under very light loads. Similarly, for $K \approx \infty$, the influence of output capacitances on the ZVS region is depicted for different ω_n values in Figure 7(c). It shows that decreasing ω_n (increasing output capacitance) narrows the ZVS region. This is because the minimum current required to ensure ZVS rises as the capacitance value increases. Obviously, a good designer can keep the converter in the ZVS region by determining an appropriate inductor under certain operating conditions.

Table 2. Main requirements of the DAB converter to be designed

Parameter	Symbol	Value	Unit
Input voltage	V_{1min}	36	V
	V_{1max}	60	
Output voltage	V_o	5	V
Rated power	P_{2max}	50	W
Rated output current	I_{omax}	10	A
Switching frequency	f_s	50	kHz
Maximum phase-shift ratio	d_{max}	0.4	-
Peak-to-peak voltage ripple	Δ_{Vo}	100	mV

Table 3. Calculated circuit parameters for the designed DAB converter

Parameter	Symbol	Value	Unit
Transformer turn ratio	N	9.6	-
Total inductance value	L	82.944	μH
Output filter capacitance value	C_o	711.11	μF

PRACTICAL DESIGN CONSIDERATIONS

Design Guidelines

The main design parameters are taken as the input and output voltages and the maximum power. The switching frequency is another known parameter, and its optimum value is chosen in line with the maximum volume and total loss limits of the converter. Taking these given parameters into consideration, the turn ratio N, inductor L, and output filter capacitor C_o need to be determined, respectively.

Two different design strategies have been presented in [20]: the first approach aims to increase the ZVS operating range to achieve good efficiency over a wide power range, and the second one aims to increase the converter efficiency at full load. In both approaches, the input voltage is considered constant, and how to calculate the inductance value that allows maximum power transfer is explained. A design procedure is not, nevertheless, presented for selecting the output capacitor. In this study, the first strategy is followed, and differently from [20], the proposed design steps address critical parameter selections in determining the inductance value for variable input voltage. The design equations for the output filter capacitor are also presented. The basic requirements for exemplary design are given in Table 2. Our example is set up on a 50W converter whose input voltage varies in the range of $36\mathrm{V} < V_1 < 60\mathrm{V}$. The output voltage is assumed to be constant and is selected as $V_2 = 5\mathrm{V}$. A simple design procedure for a wide input voltage range can be given as follows:

Step 1: Calculation of N transformer turn ratio.

As seen in Figure 7(a), an ideal design can be realized for $m = 1$ when the input voltage is constant. This is because the converter always remains in the ZVS region for the entire power range. However, if the input voltage is considered to vary between two distinct extremes, then operating points other than $m = 1$ also occur. To achieve an efficient conversion over a wide power range, the value of m should be kept close to 1. Thus, to determine the turn ratio, the input voltage can simply be taken as the arithmetic average of two extreme points, i.e. $V_1^* = \frac{V_{1min}+V_{1max}}{2}$. Then, the turn ratio is calculated for $V_1^* = 48$V. Using Eq. (1), we obtain

$$N^* = \left.\frac{V_1}{V_2}\right|_{V_1=V_1^*} \tag{47}$$

The calculated turn ratio $N^* = 9.6$ causes the converter to operate in boost mode for the input voltage range $36\text{V} < V_1 < 48\text{V}$ while the buck operation mode occurs for $48\text{V} < V_1 < 60\text{V}$. In this context, the voltage conversion ratio changes in the range of $0.8 < m < 1.333$. The designer can modify the value of N^* to boost the converter efficiency according to the operating conditions. It will be discussed in detail later in the next subsection.

Step 2: Calculation of L inductance value.

To ensure ZVS over a wide power range, as much energy as possible should be stored in the inductor; hence, the value of L should be as high as possible. The phase-shift ratio should also be selected high to increase the ZVS operation range on the one hand and to allow maximum output power on the other. From Eq. (18), the maximum value of L can be calculated as

$$L = \left.\left(\frac{NV_1V_2}{2f_sP_{2max}}d_{max}(1-d_{max})\right)\right|_{\substack{N=N^*\\V_1=V_{1min}}} \tag{48}$$

where V_1 is taken as V_{1min} to prevent an increase in the RMS and peak currents of the converter. Theoretically, the highest value of d is 0.5, but d_{max} is never chosen as 0.5. To establish a linear relationship between the phase-shift ratio and the output current or voltage, d_{max} is taken as 0.4 or even 0.35. Consequently, the maximum of L is calculated as 82.944μH.

Step 3: Calculation of C_o filter capacitance value.

As stated previously in the output ripple analysis (for a resistive load), the minimum value of the output filter capacitor that will allow the desired ripple voltage is calculated as

$$C_o \geq \frac{\Delta Q}{\Delta V_o} \tag{49}$$

It is known that the converter can operate in either buck, main, or boost operation modes depending on the selected turn ratio N^* and the input voltage range. The purpose of the design is to keep the output voltage ripple at a maximum of ΔV_o, regardless of all these operation modes. This condition can be satisfied for $\Delta Q = \Delta Q_{max}$, where $\Delta Q_{max} = \max(\Delta Q^*_{buck}, \Delta Q^*_{main}, \Delta Q^*_{boost})$. Using Eqs. (33), (34), and (35), we obtain

$$\Delta Q^*_{buck} = \Delta Q_{buck}\Big|_{\substack{N=N^*\\V_1=V_{1max}\\d=d_{max}}},\quad \Delta Q^*_{main} = \Delta Q_{main}\Big|_{\substack{N=N^*\\V_1=V_{1max}\\d=d_{max}}}$$
$$\Delta Q^*_{boost} = \Delta Q_{boost}\Big|_{\substack{N=N^*\\V_1=V_{1min}\\d=d_{\max}}} \tag{50}$$

where ΔQ^*_{buck}, ΔQ^*_{main}, and ΔQ^*_{boost} are the calculated values for the worst cases of the input voltage. ΔQ^*_{buck}, ΔQ^*_{main}, and ΔQ^*_{boost} are obtained 62.5μC, 71.111μC, and 66.694μC, respectively. Then, ΔQ_{max} becomes equal to 71.111μC. As a result, to keep the voltage ripple across C_o below 100mV, the minimum value of C_o is calculated from Eq. (49) as 711.11μF.

The circuit parameters of the designed converter are presented in Table 3. They will be used in later simulation studies.

Computational Analysis

This section presents some computational analysis on the ZVS boundaries of primary and secondary side bridges and steady-state values for the designed converter. First, the minimum operating conditions to operate both bridges within the ZVS region have been investigated for two extreme points of the input voltage. Whether the relevant bridge will perform soft-switching is determined by the boundary load condition, and if the converter operates under heavy load conditions, then both bridges always run in the ZVS region. In the case of $m = 0.8$, the phase-shift angle for the boundary load condition is calculated as $\phi = 0.3142$ from Eq. (11), and thus the phase-shift ratio $d = \phi/\pi$ becomes equal to 0.1. Similarly, using Eq. (13), the boundary load condition for $m = 1.333$ occurs at $\phi = 0.3924$ or $d = 0.1249$. Accordingly, the heavy load conditions arise when $d > 0.1$ and $d > 0.1249$ for $m = 0.8$ and 1.333, respectively. Further, the normalized average output currents for the heavy load conditions $d > 0.1$ and $d > 0.1249$ are respectively calculated as $\overline{I}_2 > 0.2827$ and $\overline{I}_2 > 0.3434$ from Eq. (42). This means that the average load current from Eq. (26) or $I_o = NI_n\,\overline{I}_2$ (pu) should not fall below 6.249A for $m = 0.8$ and 4.554A for $m = 1.333$ to operate the converter in the ZVS region. If $I_o < 6.249$A for $m = 0.8$, the light load condition occurs, and the primary side bridge performs hard-switching. Similarly, the light load condition occurs when $I_o < 4.554$A for $m = 1.333$, and the secondary side bridge performs hard-switching. Table 4 summarizes the minimum operating conditions to remain the primary and secondary bridges in the ZVS region for two extreme points of the input voltage.

Second, some open-loop simulations have been realized to evaluate the calculated steady-state values. Figure 8 shows the open-loop current and voltage waveforms for ($m = 0.8$), 1, and 1.333, respectively. The converter was operated under

Table 4. Minimum operating conditions to operate both bridges within the ZVS region for two extreme points of the input voltage

Parameter	Value	
V_o	5V	
V_1	36V	60V
m	1.333	0.8
Operating mode	Boost	Buck
d	>0.1249	>0.1
$\overline{I}_2$ (pu)	>0.3434	>0.2827
I_o	>4.554A	>6.249A
Bridge in the ZVS region	Primary side	Secondary side

Table 5. Computational and simulation results of steady-state values for m = 0.8, 1, and 1.333

Operating conditions	V_1	60V	V_o	5V
	N	9.6	m	0.8
	P_o	50W	d	0.1744
Parameter	**Calculated values**		**Simulated values**	
I_1	0.538A		≈0.552A	
I_2	1.733A		≈1.726A	
ΔV_o	≤100mV		≈21.45mV	
Operating conditions	V_1	48V	V_o	5V
	N	9.6	m	1
	P_o	50W	d	0.2354
Parameter	**Calculated values**		**Simulated values**	
I_1	1.362A		≈1.358A	
I_2	1.362A		≈1.366A	
ΔV_o	≤100mV		≈33.28mV	
Operating Conditions	V_1	36V	V_o	5V
	N	9.6	m	1.333
	P_o	50W	d	0.4
Parameter	**Calculated values**		**Simulated values**	
I_1	2.459A		≈2.454A	
I_2	1.591A		≈1.584A	
ΔV_o	≤100mV		≈80.07mV	

the rated load condition (I_o = 10A), and the phase-shift ratio corresponding to each m was calculated from Eq. (18) as d = 0.1744, 0.2354, and 0.4, respectively. The simulated waveforms in Figure 8 are quite analogical compared to the basic theoretical waveforms. The instantaneous values I_1 and I_2 of the inductor current are calculated by Eqs. (8) and (9), and they match the simulated values. It is also seen that the peak-to-peak voltage ripple ΔV_o is less than 100mV for each operating mode. The comparison of computational and simulation results is presented in Table 5.

Transformer Turn Ratio Trade-Offs

The transformer turn ratio is a key factor in determining the operation modes (buck or boost modes) in a DAB converter, as seen in Eq. (1). When considering the entire power range, the turn ratio also plays a vital role in characterizing the voltage and current profiles across the total inductor. The inductor voltage is the difference between the primary and secondary voltages of the transformer, and the slope

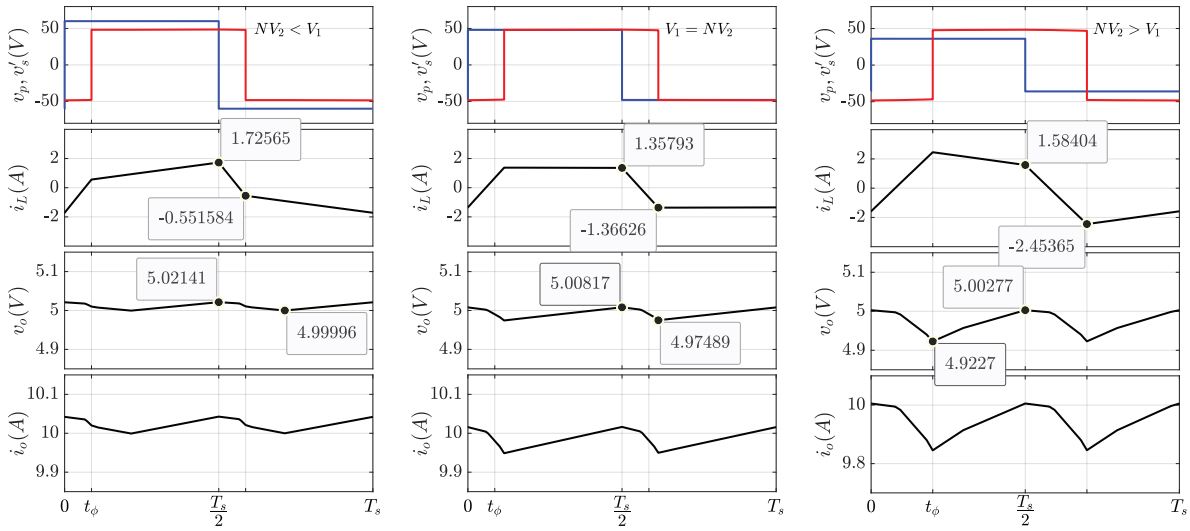

Figure 8. Simulated open-loop current and voltage waveforms under the rated load condition for **(a)** Buck (m = 0.8), **(b)** Main (m = 1), and **(c)** Boost (m = 1.333) operation modes.

of the inductor current is defined by Eq. (2). As shown in Figure 2, when $V_1 = NV_2$, the slope becomes zero, and the inductor current always changes in a trapezoidal profile. When $V_1 > NV_2$ or $V_1 < NV_2$, the inductor current varies with the positive or negative value of the slope, and thus the current profile contains spikes or peak points as illustrated in Figure 3 and Figure 4. The value of the peak currents increases dramatically when the mismatch of the voltages on both sides of the transformer heightens to a considerable degree. The current profile with large peaks increases the RMS value of the current across the primary and secondary sides. The RMS value of the primary side current can be calculated using the waveform of i_L in Figure 3(a) and expressed as

$$I_{p,rms} = \sqrt{\frac{I_1^2 + I_2^2 + I_1 I_2 (1 - 2d)}{3}} \tag{51}$$

and the RMS value of the secondary side current is $I_{s,rms} = NI_{p,rms}$. To illustrate the relationship between the turn ratio and the RMS value of current, three designs meeting the main requirements in Table 2 but with distinct turn ratios are considered. The first one is the converter designed in the previous subsection, and $V_1^* = 48$V, $N^* = 9.6$. The second and third designs are respectively realized for $V_1^* = 40$V and $V_1^* = 56$V, and the turn ratios N^* are found as 8 and 11.2. Also, the other circuit parameters for the second and third designs are $L = 69.12\mu$H, $C_o = 871.2\mu$F and $L = 96.768\mu$H, $C_o = 1500\mu$F, respectively.

The change in the primary RMS current of each design through the entire power range is shown separately in Figure 9 for three input voltages (V_{1min}, V_1^*,V_{1max}). The minimum RMS current profile in the given designs occurs for $V_1 = NV_2$ or $m = 1$ through almost the entire power range, and this profile decreases proportionally as the value of N increases. Moreover, depending on the increasing N value, the RMS current profile for the maximum value $V_{1max} = 60$V of the input voltage approaches the minimum current profile. The maximum RMS profile occurs when the input voltage tends to its minimum value $V_{1min} = 36$V, and thus the RMS

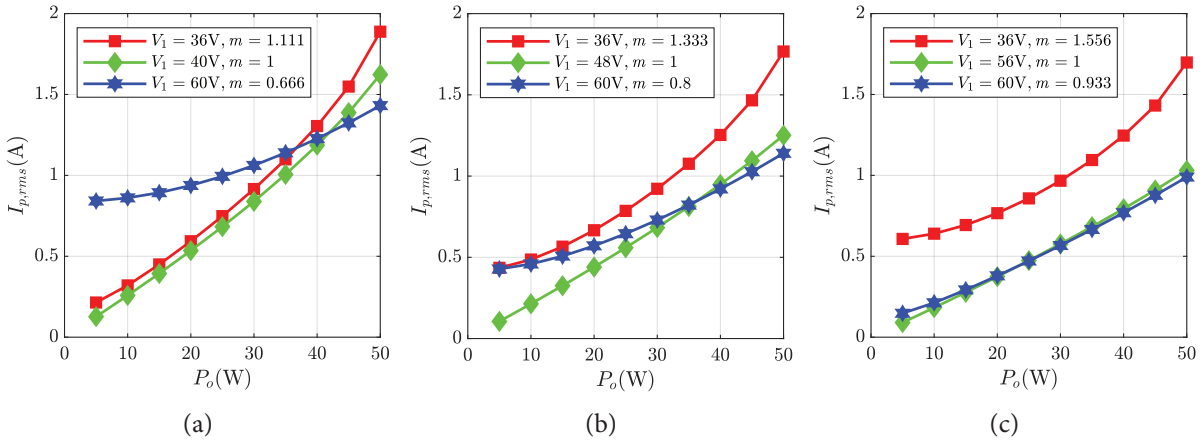

Figure 9. Change of the primary RMS current for three different transformer turn ratios: **(a)** $N = 8$, **(b)** $N = 9.6$, **(c)** $N = 11.2$.

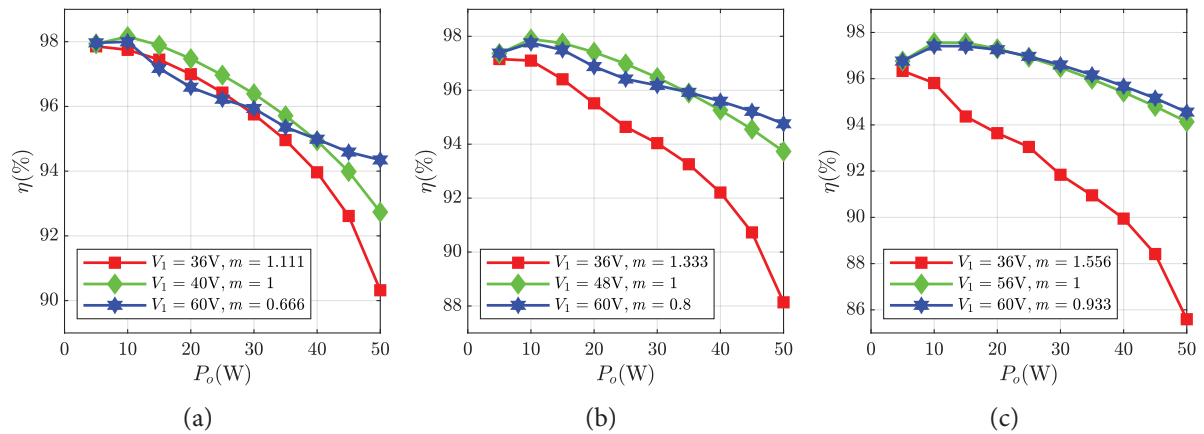

Figure 10. Efficiency curves for three different transformer turn ratios: **(a)** $N = 8$, **(b)** $N = 9.6$, **(c)** $N = 11.2$.

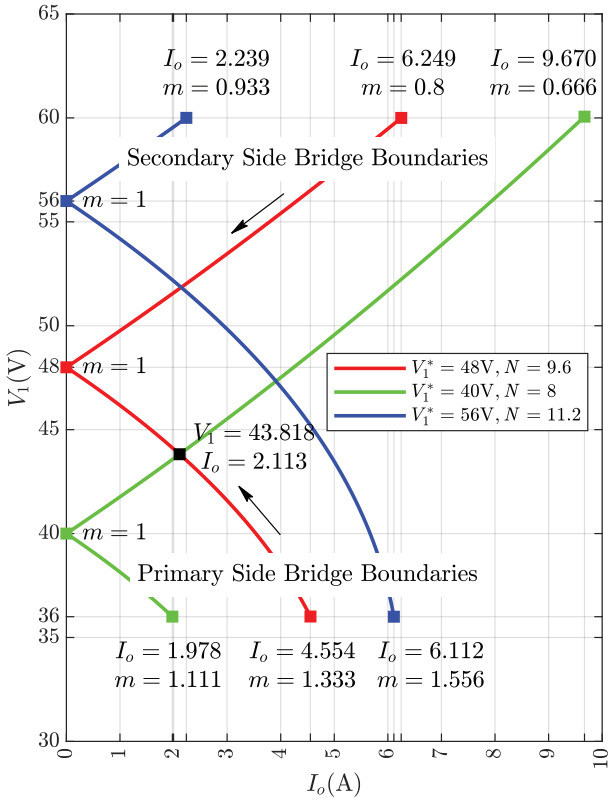

Figure 11. Variation of the minimum average output current required for ZVS to the input voltage.

currents increase significantly. This is an important trade-off to consider when determining the transformer turn ratio. A high RMS current profile results in increased power losses in the transformer. For a given core size, higher voltage or current increases core losses, and a saturation problem may also be observed. Higher current leads to larger resistive losses, possibly leading to more heating in the windings. All these negatively affect the overall efficiency of the converter. Figure 10 depicts the converter efficiencies at similar operating conditions for these three designs. The efficiency analysis was conducted using Simcape Electrical Toolbox in Matlab. The dead time is taken as 100ns. As expected, the simulated efficiency curves change inversely with the RMS current profiles in Figure 9.

The transformer turn ratio can also be used to configure the ZVS operating region of the converter. The minimum average output current that allows the converter to operate in the ZVS region decreases as the voltage conversion ratio m approaches one. This variation for the first design (N = 9.6) is depicted with red curves in Figure 11. For the other two designs (N = 8 and N = 11.2), they are plotted on the same figure with green and blue curves, respectively. By examining Figure 11, it can be concluded that the designer can modify the value of V_1^* depending on the operating conditions to keep the converter in the ZVS region. For example, if the converter operates mostly at low input voltages under different load conditions throughout the entire operating period, then V_1^* can be chosen closer to the minimum input voltage. Such a case is presented in Figure 11 with green curves for V_1^* = 40V. Thus, the required load current to stay in the ZVS region further reduces for 36V < V_1 < 43.818V when compared to the first design (i.e., the ZVS operation range widens); however, the minimum load current increases for input voltages higher than V_1 = 43.818V (i.e., the ZVS operation range narrows). On the contrary, as the turn ratio increases, this time, the ZVS operating range becomes wider for the inputs close to the maximum input voltage (see blue curves in Figure 11). The point to be noted here is that high RMS current levels will occur at around the minimum values of the input voltage due to the increasing turn ratio, as deduced from Figure 9. The designers are advised to consider this trade-off when determining the turn ratio.

The above considerations highlight the importance of determining an optimum transformer turn ratio based on operating conditions. The trade-offs associated with selecting an optimum turn ratio affect various aspects of converter performance, including RMS current levels, efficiency, heating, and ZVS operating range.

Practical Challenges

In real-world applications, several practical challenges can arise due to component non-idealities, high-frequency transformer design, sensing mechanism noise, thermal management, and switch current ratings. These significantly affect the performance, reliability, and longevity of the converter. The following introduces a brief description of these difficulties:

Component Non-Idealities: All electronic components such as resistor, capacitor, and semiconductor devices can never exhibit ideal theoretical behavior. Non-ideal behaviors typically stem from manufacturing imperfections, nonlinear characteristics, and environmental factors. Tolerance, aging, parasitic effects, and temperature dependence of components are only some of their non-idealities.

High-Frequency (HF) Transformer Design: HF transformer design involves unique challenges due to the complex interplay of electrical, magnetic, thermal, and mechanical factors. At high frequencies, core losses (hysteresis and eddy current losses) reduce efficiency and generate heat. Hysteresis losses can be mitigated by using core materials, such as ferrites or nanocrystalline alloys. Similarly, using laminated or powdered cores can reduce eddy current losses. Ferrite cores are commonly preferred in high-frequency designs because of their high resistivity. High-frequency currents also tend to increase winding losses (skin and proximity effects). The skin effect causes a decrease in the effective cross-sectional area and an increase in the AC resistance. To reduce losses due to the skin effect at high frequencies, Litz wire can be used instead of solid copper wire in the windings. The proximity effect causes

non-uniform current distribution and additional losses. This can be somewhat reduced at high frequencies by optimizing winding geometry or using interleaved windings. The transformer parasitic capacitances (inter-winding capacitance and winding self-capacitance) result in unwanted resonances and signal distortion, and their effects become more intense at high-frequency operation. To minimize the effects of parasitic capacitances, shielding layers between windings and techniques like sectional winding can be used. Finally, high-frequency transformers generate electromagnetic interference (EMI), which can disrupt nearby electronics and violate regulatory and safety standards. Shielding and filtering techniques can be implemented to reduce EMI.

Sensing Mechanism Noise: Measuring physical quantities such as current and voltage is critical to all power electronics circuits, but the accuracy and reliability of measurements can degrade when they are subject to noise and interference. Sensing mechanisms are susceptible to noise from various sources, such as thermal noise, shot noise, and EMI. Quantization noise is another factor that occurs during the process of converting an analog signal into digital form and limits measurement resolution and accuracy, especially in high-precision applications. Besides, environmental interference like temperature fluctuations, humidity, or vibrations and cross-talk between different sensor lines or components can cause noise or drift in sensor readings.

Thermal Management: Many electronic components, especially semiconductor devices, generate considerable heat during operation at high frequencies under high power. The produced heat should be effectively dissipated without allowing critical components to exceed their thermal limits. Otherwise, it can lead to failure, reduced efficiency, and even permanent damage. Therefore, it is critical to balance heat generation and dissipation to ensure safe operation. The heat dissipation method varies depending on power rating, design dimensions, and design purposes, but it generally involves using passive methods like heat sinks or active methods like fans or liquid cooling systems.

Switch Current Rating: To operate a switch within its safe limits, it is also necessary to consider its voltage and current ratings along with its power dissipation capacity and thermal management. The current rating of a DAB converter is determined by the total inductance design, and real designs usually focus on this aspect. The maximum value of the inductance that will provide the maximum output power was obtained in the Design Guidelines subsection. Choosing a smaller inductance than its maximum value brings a high current impact on the transformer and switches. This is illustrated in Figure 12, which gives the variations of the primary and secondary side RMS currents to the total inductance. The simulation results are obtained for $N^* = 9.6$ and three switching frequencies (15, 30 and 50kHz) at the maximum output power, considering only

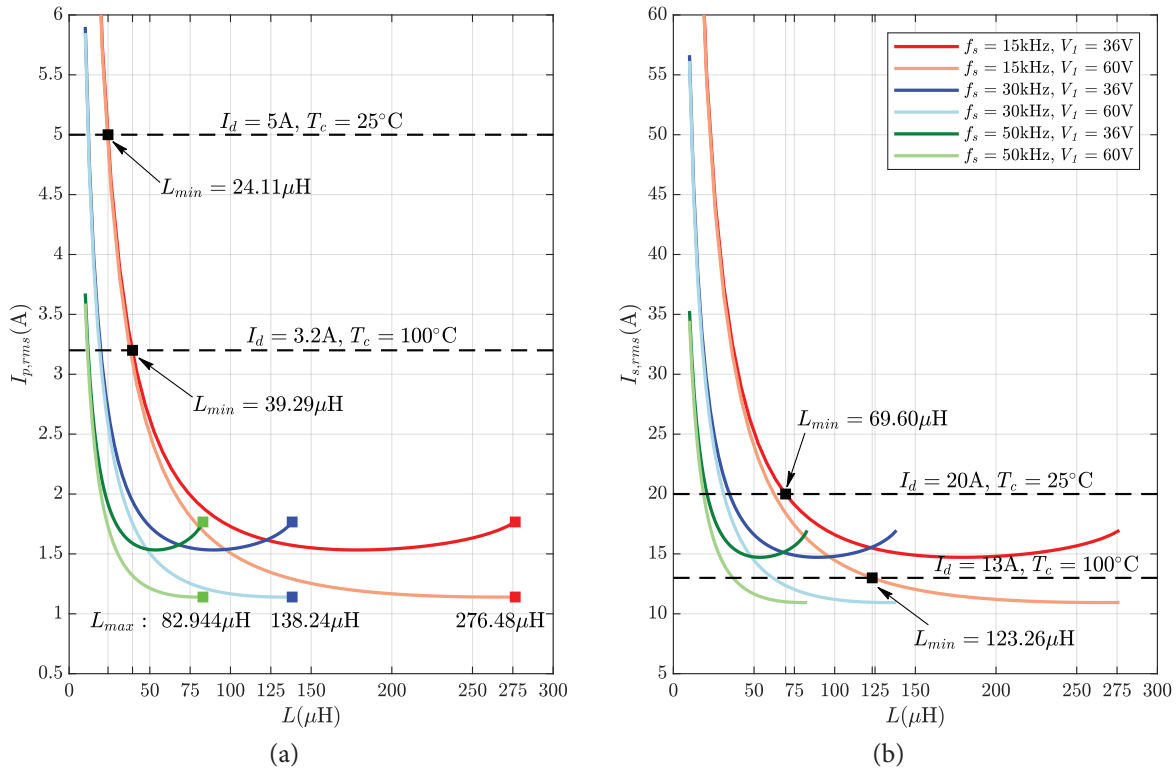

Figure 12. Variations of the RMS currents to the total inductance; (a) for the primary side bridge, (b) for the secondary side bridge.

the two extreme points of the input voltage. As can be seen, the maximum value of the inductance increases to ensure the maximum output power at low switching frequencies. In fact, Figure 12 also refers to the current rating limits within which a switch can operate without causing damage or failure. For example, let IRF830A Power MOSFET for the primary side bridge and IRFP460B Power MOSFET for the secondary side bridge be selected as the switching devices. Both MOSFETs can withstand a voltage of 500V and exhibit a good voltage-blocking capability for the present design. On the other hand, the IRF830A can handle continuous drain currents of 5A at T_C = 25°C and 3.2A at T_C = 100°C at the most. These currents for the IRFP460B are 20A and 13A at T_C = 25°C and 100°C, respectively. T_C is the case temperature of MOSFET. These current endurances are relatively low, and therefore the inductance value should be selected carefully. For this, the current limitations of MOSFET devices are also shown in Figure 12. If the primary side MOSFET is switched at 15kHz, the inductance must be between 24.11μH and 276.48μH to safely meet the 50W power requirement. Under poor thermal management, device failures may occur for the inductance values selected between 24.11μH and 39.29μH. Thus, it is recommended not to choose a small inductance for low switching frequencies. Similarly, if the secondary side MOSFET is operated at 15kHz, the current exceeds the threshold when L < 69.6μH, and it is damaged during maximum power transmission. More importantly, the device is likely to fail under bad thermal management, especially for input voltage V_1 = 36V. This issue can also be experienced at other switching frequencies. Thus, to guarantee safe operation, it is recommended to select a MOSFET with a continuous drain current greater than 16.96A at T_C = 100°C.

CONTROL STRATEGIES

The study discusses five different PI-based control strategies, namely TVL, LCFF, e-MPS, DP, and VDP controls, as well as MPS control. These are briefly examined for unidirectional power flow, where the secondary side bridge feeds a passive load. Figure 13 shows the block diagram of all these control schemes.

Traditional Voltage Loop (TVL) Control: The block diagram of the TVL control scheme is shown in Figure 13(b). This traditional scheme comprises a simple voltage loop. The desired phase-shift ratio is generated from the proportional gain of the output voltage error. The integral gain can be used to cope with the nonlinearities in the relationship and to improve the generated phase-shift ratio. Thus, the desired phase-shift ratio d^* is directly produced as

$$d^* = k_p(v_o^* - v_o) + k_i \int (v_o^* - v_o)\, dt \qquad (52)$$

where v_o^* is the desired output voltage. k_p and k_i are the proportional and integral coefficients, respectively. In this scheme, only measuring the actual output voltage is sufficient to achieve voltage control. The TVL control can exhibit a fast dynamic response to the output voltage step change, however, the response is substantially slower when there is a change in the load current.

Load Current Feed-Forward (LCFF) Control: To eliminate the slow load transient response during voltage mode control, the TVL control scheme can be improved by combining it with the load current feedforward. This scheme has a cascade structure that consists of an inner current loop and an outer voltage loop. The block diagram of the LCFF control is given in Figure 13(b), where the desired phase-shift ratio is generated as

$$d^* = ki_o + k_p(v_o^* - v_o) + k_i \int (v_o^* - v_o)\, dt \qquad (53)$$

where k is the feedforward gain. It is clear from Eq. (53) that the load current needs to be measured as well as the output voltage to implement it. With the LCFF control, a better dynamic response can be achieved under load variations compared to the TVL control.

Model-Based Phase-Shift (MPS) Control: According to the MPS control [46,47], the desired phase-shift ratio is derived from Eq. (24) as

$$d^* = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2f_s L v_o^*}{N v_1 R_L}} \qquad (54)$$

To evaluate Eq. (54), the load resistance should be estimated online. Simply, it is identified as $R_L = v_o / i_o$ [50], and the substitution of it into Eq. (54) leads to

$$d^* = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2f_s L v_o^*}{N v_1} \frac{i_o}{v_o}} \qquad (55)$$

It is obvious from Eq. (55) that the desired phase-shift ratio is dependent on the inductor L, the transformer turn ratio N, and the switching frequency f_s. Thus, to calculate the value of d^* with high accuracy, these parameters should be extremely accurate. Further, it is also necessary to sense the load current and input voltage precisely. Otherwise, all of them cause the phase-shift ratio to be incorrect and hence the output voltage control to deteriorate. The block diagram of the MPS control scheme is given in Figure 13(c). In practice, the large output filter capacitor prevents the output voltage from varying immediately when the load resistor changes. This slow rate of change in the voltage affects the estimation performance of the load resistance. Thus, the MPS control can exhibit a relatively poor dynamic response to the load current changes, particularly step changes.

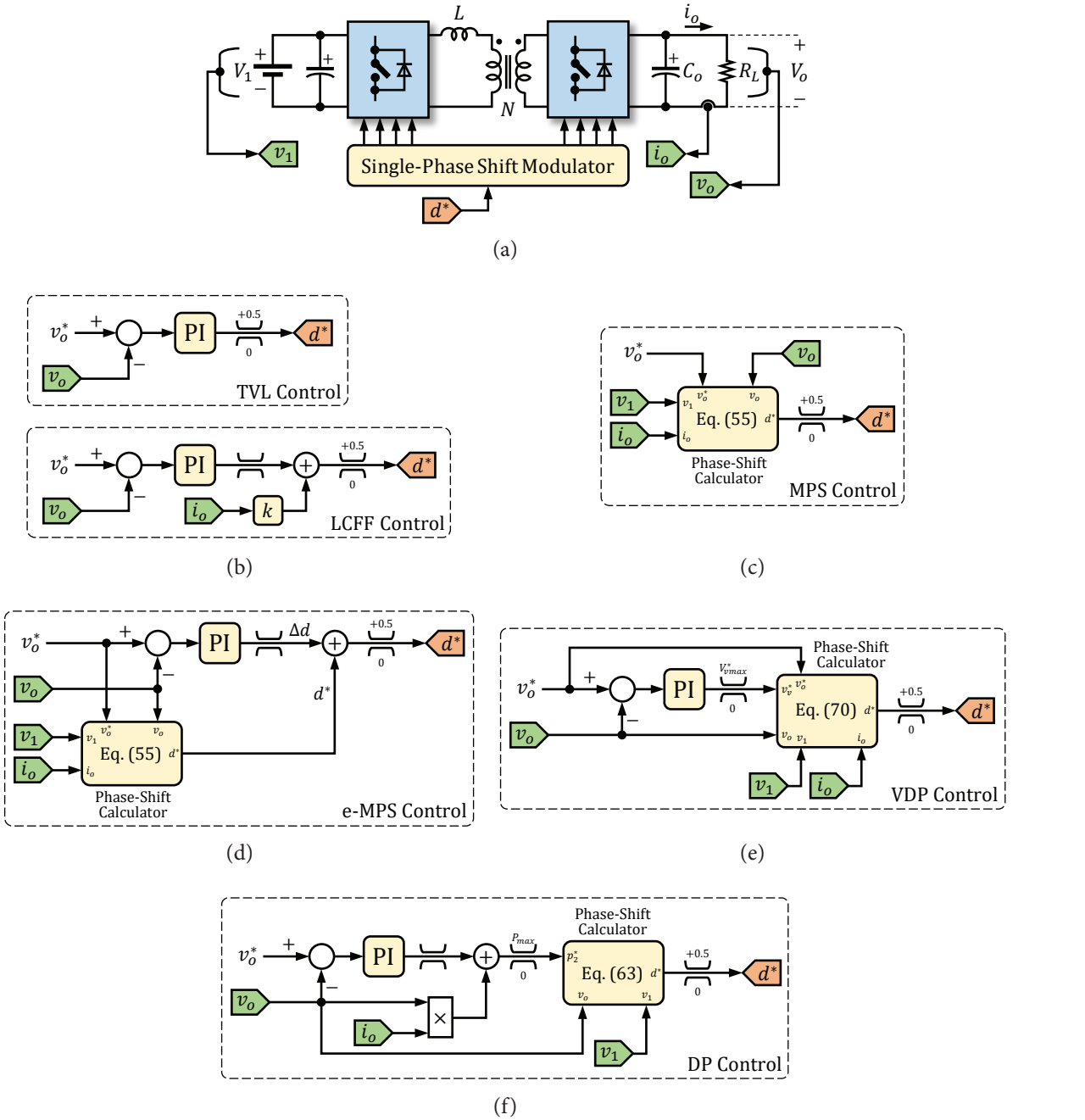

Figure 13. Control schemes for DAB converter; **(a)** DAB converter and measurement points, **(b)** TVL and LCFF control, **(c)** MPS control, **(d)** e-MPS control, **(e)** VDP control, **(f)** DP control.

To improve the dynamic performance, especially at light loads, a PI controller is adopted for this scheme [46,47], as given in Figure 13(d). The output of the controller Δd is defined by

$$\Delta d = k_p(v_o^* - v_o) + k_i \int (v_o^* - v_o)\, dt \tag{56}$$

and the enhanced phase-shift ratio is then $d = d^* + \Delta d$, where $d \in [0,0.5]$. For the e-MPS scheme, the load resistance can be estimated from Eq. (24) as follows [46]:

$$R_L = \frac{2f_s L}{N v_1} \frac{v_o}{d_{init}(1 - d_{init})} \tag{57}$$

Combining Eq. (54) with Eq. (57) yields

$$d^* = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{v_o^*}{v_o} d_{init}(1 - d_{init})} \tag{58}$$

where d_{init} is an arbitrary initial value. In this scheme, the desired phase-shift ratio is independent of constant

parameters, and only sensing the output voltage is sufficient to estimate it. The disadvantage is that d_{init} is set arbitrarily and cannot be changed later. Thus, the PI controller should be designed more carefully to compensate for it, otherwise the incorrectly identified d^* emerges as a large error in the output.

Direct Power (DP) Control: From Eq. (20), the unified transmission power is

$$p_2 = \frac{N v_1 v_2}{2 f_s L} d(1 - |d|) \tag{59}$$

and solving Eq. (59) for the desired output power p_2^*, the desired phase-shift ratio is determined as

$$d^* = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2 f_s L}{N v_1 v_2} p_2^*} \ , & p_2^* > 0 \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{2 f_s L}{N v_1 v_2} p_2^*} \ , & p_2^* < 0 \end{cases} \tag{60}$$

As in Figure 6(a), the desired output power is,

$$p_2^* = v_o C_o \frac{dv_o}{dt} + v_o i_o \tag{61}$$

where v_o is relatively constant at steady-state, and dv_o/dt is close to zero. However, this term appears during transient states such as voltage and load variation. Generally, dv_o/dt can be approximated by $\Delta v_o / T_s$, where T_s is the sampling (or switching) period. Since the change of the output voltage along T_s is $\Delta v_o = v_o^*$ - v_o, Eq. (61) can be interpreted [48] as

$$p_2^* = v_o i_o + k_p (v_o^* - v_o) + k_i \int (v_o^* - v_o)\, dt \tag{62}$$

where the proportional controller compensates for the first term of Eq. (61), and k_p should be chosen smaller than $v_o C_o / T_s$ to guarantee stability. Moreover, to improve the dynamic performance, an integral controller is also added to this scheme. Consequently, the desired value of d for p_2^* > 0 is calculated from Eq. (60) by

$$d^* = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2 f_s L}{N v_1 v_o} p_2^*} \ , \quad p_2^* \in [0, P_{2max}] \tag{63}$$

It is clear from Eq. (63) that d^* is dependent on constant parameters, such as L, N, and f_s. It is also necessary to feed forward the load current and input voltage precisely. The block diagram of the DP control scheme is presented in Figure 13(f).

Virtual Direct Power (VDP) Control: In the VDP control [50], the unified transmission power is defined without fixed parameters L, N, and f_s. From Eq. (59), it is

$$p_2 = \frac{v_1 v_2}{2} d(1 - |d|) \tag{64}$$

and the desired phase-shift ratio is determined as

$$d^* = \begin{cases} \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{p_2^*}{v_1 v_2}} \ , & p_2^* > 0 \\ -\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{p_2^*}{v_1 v_2}} \ , & p_2^* < 0 \end{cases} \tag{65}$$

where p_2^* is the virtual desired output power. For unidirectional power flow, it is expressed as,

$$p_2^* = v_v^* i_o^* \tag{66}$$

and

$$v_v^* = k_p (v_o^* - v_o) + k_i \int (v_o^* - v_o)\, dt \tag{67}$$

$$i_o^* = \frac{v_o^*}{v_o} i_o \tag{68}$$

where v_v^* is the virtual desired output voltage, and i_o^* is the desired load current. As seen above, the virtual voltage v_v^* is generated from a PI controller. Thus, it allows us to adjust the output voltage. Substituting Eq. (68) into Eq. (66) yields

$$p_2^* = \frac{v_v^* v_o^*}{v_o} i_o \tag{69}$$

Then, the desired value d for $p_2^* > 0$ is calculated from Eq. (65) by

$$d^* = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{v_v^* v_o^*}{v_1 v_o^2} i_o} \ , \quad v_v^* \in \left[0, \frac{v_1 v_o^2}{4 v_o^* i_o}\right] \tag{70}$$

Unlike the MPSC and DPC schemes, the VDP control scheme is insensitive to the parameters L, N, and f_s. Nevertheless, it requires additional measurements for the load current and input voltage feedforward as in the others. The block diagram of the VDP control scheme is shown in Figure 13(e).

The major differences and strengths of the control strategies are summarized comparatively in Table 6. In addition, each control strategy balances the transient and steady-state performance of the converter as follows:

- PI controllers in the TVL and LCFF schemes compensate for the error between the actual and desired output voltage, and they are used to generate the phase-shift ratio directly. In the LCFF control, the closed-loop output impedance is reduced by a load current feedforward,

Table 6. General comparison of PI-based control strategies

Control strategies	Implementation complexity	Implementation cost	Robustness against parameter variation	Dynamic performance
TVLC	Very Low	Low, 1 sensor	Good	Good
LCFFC	Low	Medium, 2 sensor	Good	Better
MPSC	Low	High, 3 sensor	Poor	Poor
e-MPSC	Medium	High, 3 sensor	Good	Best
DPC	High	High, 3 sensor	Average	Good
VDPC	High	High, 3 sensor	Better	Best

thus providing a faster transient response during load current changes compared to the TVL control.

- There is no controller in the MPS scheme, and the desired phase-shift ratio is always calculated from output voltage, input voltage, and load current feedforward as well as circuit parameters. The transient and steady-state responses are highly dependent on measured quantities and circuit parameters, especially load resistor. The e-MPS scheme is an improved version of MPS control. The output of the PI controller in the e-MPS scheme is used as a correction term to enhance the calculated phase-shift ratio from the MPS scheme. Thus, the e-MPS control exhibits better dynamic performance compared to the MPS control. However, in both control schemes, a steady-state error may be observed since the desired phase shift ratio is still calculated depending on circuit parameters.
- PI controllers in the DP and VDP schemes is used to compensate for the difference between the calculation model and the physical model. The output of the PI controller in the DP scheme is used as a correction term to regulate the desired output power, and the phase-shift ratio is then estimated from this corrected output power. The calculation model is highly dependent on the measured quantities and circuit parameters, and thus this can cause a steady-state error to be observed. Finally, the VDP scheme is based on the virtual output voltage, and the phase shift ratio is estimated from this virtual voltage, which is included in the calculation and adjusted by the PI controller to obtain the desired output voltage. The dynamic performance of VDP control is free of circuit parameters, but the calculation model is affected by sampled quantities.

SIMULATION RESULTS

Some simulation studies will now be presented to investigate and compare the dynamic performance of the given control strategies. To make a fair comparison, all controller parameters are optimized using Artificial Rabbits Optimization (ARO) algorithm developed in [61]. The ARO is a bio-based metaheuristic algorithm inspired by the survival strategies of rabbits in nature. Compared with some classical and latest optimizers, it generally performs better in solving benchmark functions and engineering problems. It has many superiorities, such as faster convergence, lower computational demand, and higher accuracy. In this study, the ARO algorithm is used to find the controller parameters that minimize the integral time absolute error (*ITAE*) performance criterion:

$$ITAE = \int t|e(t)|\,dt \tag{71}$$

where e is the error signal. In the simulations, the control sampling time is chosen to be equal to the switching frequency, that is, the phase-shift ratio is updated at the end of each switching period. The optimized controller parameters for each control scheme are given in Table 7.

Some performance metrics, such as settling time t_s, percentage overshoot M_p, steady-state error e_{ss}, output voltage ripple at steady-state ΔV_o, and *ITAE* index, will be used to compare the transient and steady-state responses of control strategies. The performance comparisons will be performed for step variations in input voltage, load, and output voltage. These case studies are given as follows:

Case 1: The first case study is conducted to investigate the dynamic performance of the control strategies under

Table 7. Optimized controller parameters for the given control strategies

Parameters	TVLC	LCFFC	MPSC	e-MPSC	DPC	VDPC
k_p	0.2222	0.3282	-	0.7524	95.0222	3.1027
k_i	706.9534	697.1387	-	32.75	34.4461	13103
k	-	0.0122	-	-	-	-

the load step changes. The simulation parameters are set as V_1 = 48V, V_o^* = 5V, and R_L = 0.5Ω. Initially, the converter is operated under rated power. The load resistance steps from 0.5 to 1Ω at t = 0.01s, and conversely at t = 0.03s. Figure 14 shows the output voltage and current responses for each control scheme. The transient response characteristics of the output voltage during start-up process are given in Table 8. Similar transient response and steady-state characteristics during load changes are also presented in Table 9.

From Table 8, the best transient response during start-up process is achieved by the LCFF control with a settling time of 0.521ms. While the VDP control provides the second-best response with an overshoot of 4.599%, the longest settling time also seems to be in the MPS control. From Table 9 and Figure 14, the e-MPS control exhibits the fastest dynamic performance during load step changes compared to the others. The largest overshoot and settling time exist in the TVL control, followed by the MPS and LCFF controls, respectively. The dynamic performance of the DP control

Table 8. Obtained transient response characteristics during start-up process

	TVLC	LCFFC	MPSC	e-MPSC	DPC	VDPC
Overshoot, M_p(%)	0.389	**0.712**	0.079	6.770	0.278	4.599
Settling Time, t_s (ms)	0.741	**0.521**	1.521	0.789	0.781	0.670

Table 9. Obtained transient response and steady-state characteristics during load current step changes

Load Current		TVLC	LCFFC	MPSC	e-MPSC	DPC	VDPC
10A to 5A	M_p (%)	10.250	6.187	5.372	**3.070**	5.563	5.691
	t_s (ms)	0.599	0.420	0.699	**0.026**	0.075	0.146
	e_{ss} (mV)	0	0	8.164	0.425	0.398	**0**
	ΔV_o (mV)	18.27	18.27	18.15	18.15	18.27	**18.28**
	$ITAE$ ($\times 10^{-6}$)	1.988	1.125	4.686	0.267	0.328	**0.601**
5A to 10A	M_p (%)	9.193	6.270	6.127	**3.999**	6.026	6.184
	t_s (ms)	0.771	0.611	0.651	**0.041**	0.291	0.112
	e_{ss} (mV)	0	0	15.003	0.277	5.841	**0**
	ΔV_o (mV)	59.95	59.95	59.21	59.94	59.59	**59.87**
	$ITAE$ ($\times 10^{-6}$)	5.844	3.281	8.103	0.256	3.499	**0.991**

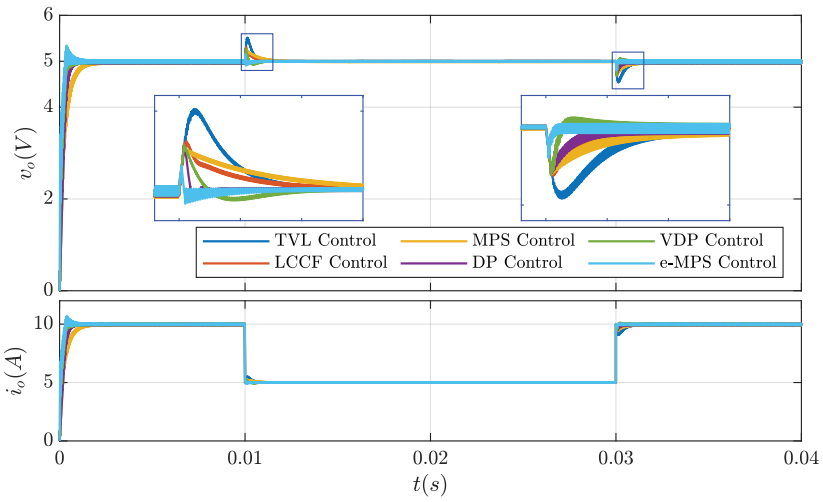

Figure 14. Simulated responses of output voltage and current during load step changes.

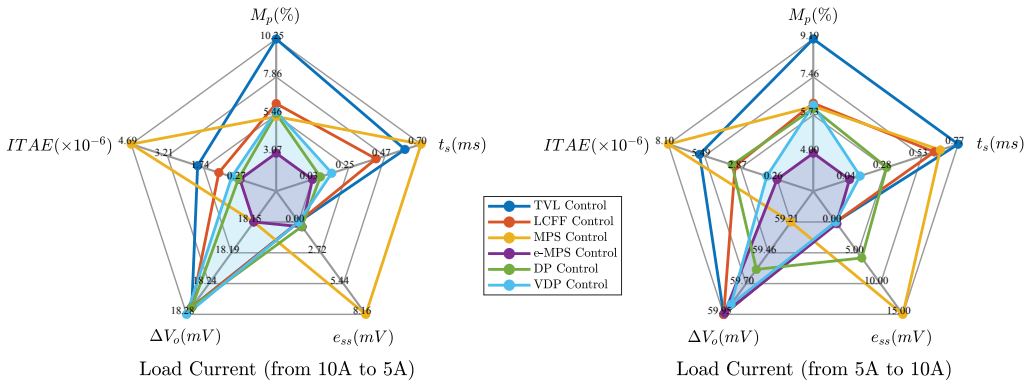

Figure 15. Spider charts for performance comparison of control techniques under load current step changes.

during the load change from 10A to 5A is quite good, while it could not exhibit a similar performance as expected in the load change from 5A to 10A. However, these two responses are still better than those of the TVL, LCFF, and MPS controls. As a result, the best transient responses have been achieved by the e-MPS and VDP controls, respectively. All control strategies have almost the same peak-to-peak ripples (≈ 18mV and ≈ 59mV for each step change, respectively) in the output voltage. It is further seen from Table 9 that the VDP control has better steady-state performance than other control methods when the *ITAE* index and steady-state error are evaluated. The obtained transient and steady-state results are represented with spider charts in Figure 15 to enable an illustrative comparison among the control strategies.

Case 2: The second case study is done to examine the dynamic performance of the control strategies under the input voltage step changes. The simulation parameters are initially set as $V_1 = 48V$, $V_o^* = 5V$, and $R_L = 0.5\Omega$. Recall that the converter is designed for input voltages within the range of $36V < V_1 < 60V$. Hence, the worst conditions, that is only two extremes of the input voltage, have been considered in the simulation. First, the input voltage steps down from 48 to 36V at $t = 0.01s$, and then steps up form 36 to 60V at $t = 0.03s$. Figure 16 shows the output voltage and current responses for each control scheme. The transient response and steady-state characteristics of the output voltage during input voltage changes are given in Table 10.

From Table 10 and Figure 16, the TVL and LCFF controls have the longest settling time of over 1ms in both the input voltage step-down and step-up conditions, and the largest overshoot rate is also observed compared to the others. Furthermore, the e-MPS control almost keeps the output voltage constant at the desired value with minimum settling time and overshoot. Consequently, it can be said that the e-MPS control exhibits an excellent dynamic performance during input voltage step changes, followed by the VDP, DP, and MPS controls, respectively. The lowest ripples in the output voltage (roughly 12mV) are observed for the TVL and LCFF controls when the input voltage is stepped down. All control strategies produce almost the same ripples around 32mV in the case that the input voltage is stepped up. Table 10 shows that the VDP control has still better steady-state performance when the *ITAE* index and

Table 10. Obtained transient response and steady-state characteristics during input voltage step changes

Input voltage		TVLC	LCFFC	MPSC	e-MPSC	DPC	VDPC
48V to 36V	M_p (%)	8.109	7.317	2.833	**2.233**	3.180	3.625
	t_s (ms)	1.292	1.472	0.252	**0.072**	0.232	0.172
	e_{ss} (mV)	0	0	51.034	6.851	23.308	**0**
	ΔV_o (mV)	12.18	12.32	118.28	121.86	119.29	**123.55**
	ITAE ($\times 10^{-6}$)	2.627	2.693	20.553	3.402	9.435	**0.102**
36V to 60V	M_p (%)	17.301	14.939	4.566	**2.699**	5.552	6.067
	t_s (ms)	0.849	1.029	0.329	**0.090**	0.073	0.130
	e_{ss} (mV)	0	0	23.676	6.654	2.173	**0**
	ΔV_o (mV)	32.25	32.25	32.84	31.76	32.23	**32.14**
	ITAE ($\times 10^{-6}$)	10.248	10.433	9.571	2.859	1.064	**0.624**

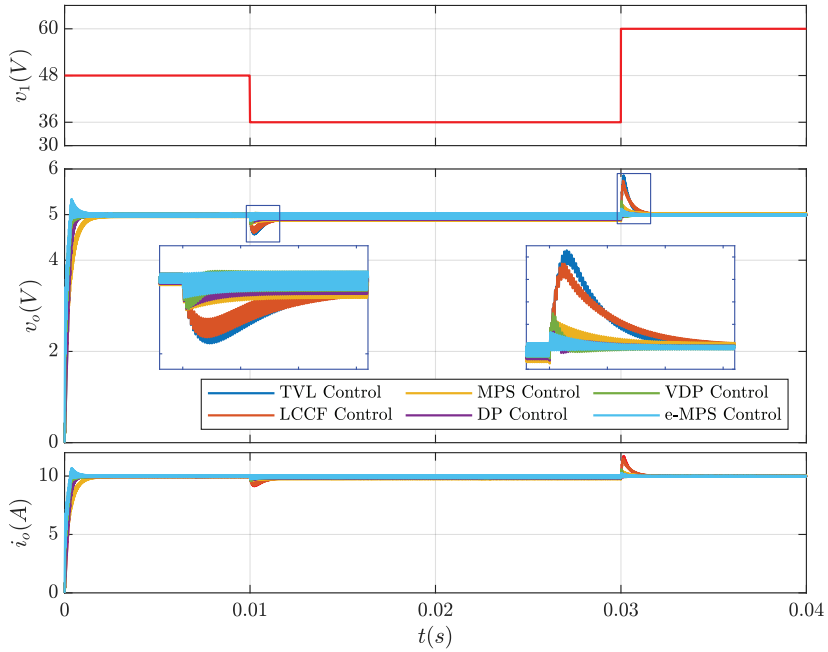

Figure 16. Simulated responses of output voltage and current during input voltage step changes.

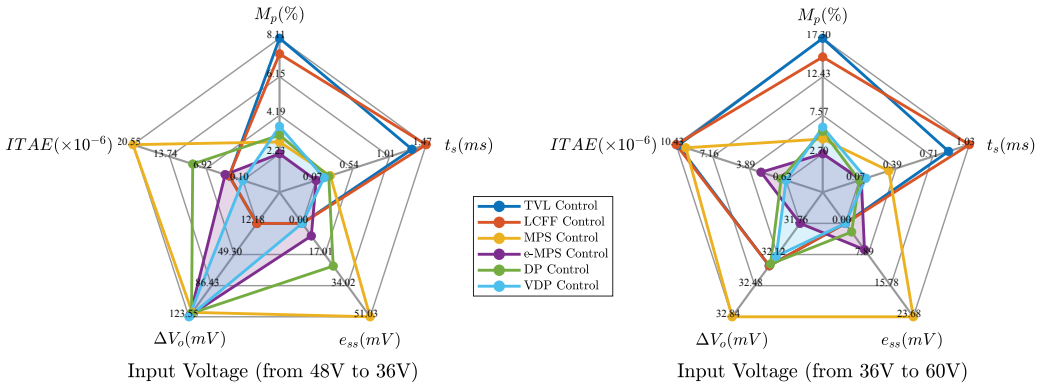

Figure 17. Spider charts for performance comparison of control techniques under input voltage step changes.

steady-state error are considered. Similar spider charts for the input voltage step changes are presented in Figure 17 to make it easy to evaluate the obtained results.

Case 3: The final case study aims to compare the dynamic performance of the control strategies under the desired output voltage step changes. The simulation parameters are now set as V_1 = 48V, V_o^* = 5V, and R_L= 1Ω. The desired output voltage steps from 5 to 7V at t = 0.01s, and subsequently steps down from 7 to 3V at t = 0.03s. Figure 18 shows the output voltage and current responses for each control scheme. The transient response and steady-state characteristics of the output voltage during its desired step changes are given in Table 11.

From Table 11 and Figure 18, the slowest transient response is obtained by the MPS control with settling times of 2.061 and 3.190ms. For the output voltage step-up condition, the fastest transient responses are achieved by the e-MPS, LCFF, VDP, TVL, and DP controls, respectively. However, for the output voltage step-down condition, the TVL, e-MPS, DP, LCFF, and VDP controls provide the fastest transient responses, respectively. As seen in Figure 18, the TVL and LCFF controls respond faster than the DP and VDP controls, but their settling times are long because of the large overshoot rate. Consequently, it can be said that the e-MPS control will be a good choice to regulate the output voltage when considering the overshoot rates. For step change from 5V to 7V, the ripple in the output voltage is

Table 11. Obtained transient response and steady-state characteristics during output voltage step changes

Output Voltage		TVLC	LCFFC	MPSC	e-MPSC	DPC	VDPC
5V to 7V	M_p (%)	3.850	2.202	0	**0.558**	0.549	0.789
	t_s (ms)	0.635	0.365	2.061	**0.191**	0.891	0.491
	e_{ss} (mV)	0	**0**	27.081	0.458	7.022	0
	ΔV_o (mV)	77.06	**77.06**	75.83	60.80	74.93	74.95
	ITAE ($\times 10^{-6}$)	3.500	**3.148**	24.244	2.433	8.201	3.887
7V to 3V	M_p (%)	6.004	2.776	0	**0.736**	3.399	5.099
	t_s (ms)	0.503	0.830	3.190	**0.750**	0.806	1.364
	e_{ss} (mV)	0	**0**	0.518	1.351	0.341	0
	ΔV_o (mV)	18.27	**18.27**	18.22	18.30	18.26	18.22
	ITAE ($\times 10^{-6}$)	6.652	**4.636**	52.405	3.452	8.933	13.314

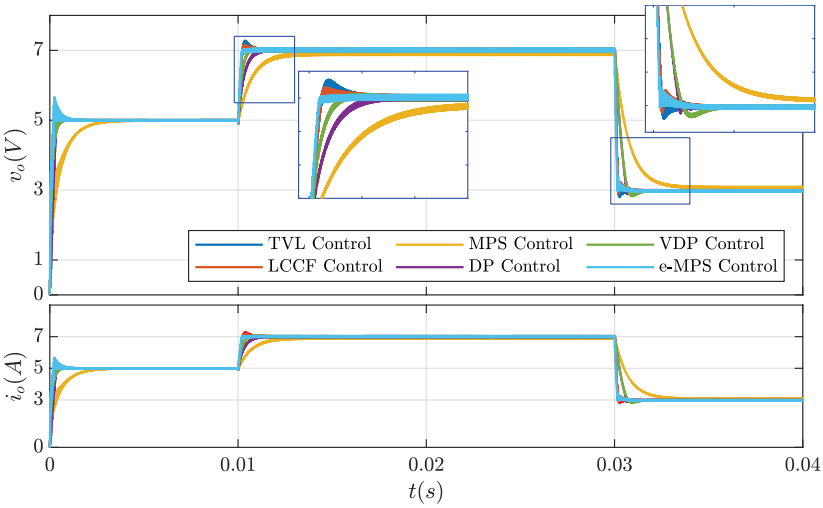

Figure 18. Simulated responses of output voltage and current during its desired step changes.

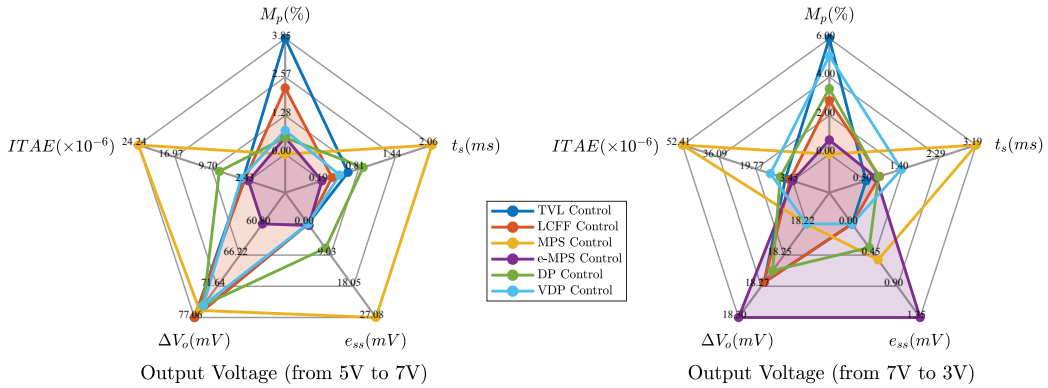

Figure 19. Spider charts for performance comparison of control techniques under output voltage step changes.

around 60.8mV for the e-MPS control, and this is relatively low compared to the ripple voltages (≈75mV) achieved for other control strategies. The output voltage ripples are almost the same for the other step change, and it is about 18mV. Table 11 shows that the LCFF control has better steady-state performance when considering the *ITAE* index and steady-state error. Similar spider charts for the output voltage step changes are presented in Figure 19.

Table 12. Overall performance comparison of control strategies

Control strategies	Start-up process	Case study–1 (load disturbance)	Case study–2 (input voltage disturbance)	Case study–3 (output voltage change)
TVLC	Good	Poor	Poor	Better
LCFFC	Best	Good	Poor	Better
MPSC	Poor	Poor	Good	Poor
e-MPSC	Good	Best	Best	Best
DPC	Good	Good	Good	Good
VDPC	Better	Better	Better	Good

According to Figures 15, 17, and 19, an overall performance comparison that rates the control strategies against each other can be given in Table 12. From Table 12, it is easy to deduce that the e-MPSC scheme exhibits the best dynamic performance among other schemes, and the second-best performance is achieved with the VDPC scheme.

CONCLUSION

This paper offers a comprehensive overview of operation modes, steady-state analyses, design recommendations, and PI-based control strategies of the single-phase-shift DAB converter. The operating modes have been distinguished in accordance with the phase-shift angle, load conditions, and voltage conversion ratio. In general, three distinct operation modes occur based on the voltage conversion ratio m, and in this study, they are called main ($m = 1$), buck ($m < 1$), and boost ($m > 1$). It is observed that various inductor current waveforms occur for the buck and boost operation modes depending on the output current, however, for the main operating mode, the inductor current is always trapezoidal regardless of the load conditions. For this reason, the buck and boost modes are further divided into two sub-operation modes by a boundary condition, and in this study, these are referred to as heavy and light load conditions. By performing a detailed steady-state analysis of the inductor current, the boundary condition, i.e., the phase-shift angle at which the boundary load condition occurs, has been obtained separately for buck and boost modes. It can be said that the studies mentioned so far are actually complementary to the previous studies in literature.

This paper also reports a detailed analysis of the output voltage ripple and a simple analysis of the soft-switching region. The output ripple analysis is important to determine the output filter capacitor. Unlike the previous studies, the ripple analysis has been realized individually for each operating mode ($m = 1$, $m < 1$, and $m > 1$) and only for heavy load conditions in this study. Furthermore, the soft-switching analysis has revealed that the ZVS is lost when the converter operates under light load conditions, and it is more possible to ensure the ZVS under heavy load conditions. Finally, this paper proposes some design recommendations that can allow a wider ZVS operation range, especially for a wide input voltage range. More importantly, it also presents a comparative analysis of optimized PI-based control strategies for a DAB converter with SPS modulation. The simulation studies show that the e-MPS control exhibits a fast dynamic response under the load current, input voltage, and desired output voltage step change conditions. The second-best performance has been achieved with the VDP control.

AUTHORSHIP CONTRIBUTION

This study emerged within the scope of the master's thesis done by U.O. at Giresun University, Department of Electrical and Electronics Engineering. All simulation studies were carried out by U.O. under the leadership of M.A.U., and all the authors equally contributed to this work.

DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest concerning the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

STATEMENT ON THE USE OF ARTIFICIAL INTELLIGENCE

Artificial intelligence was not used in the preparation of the article.

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